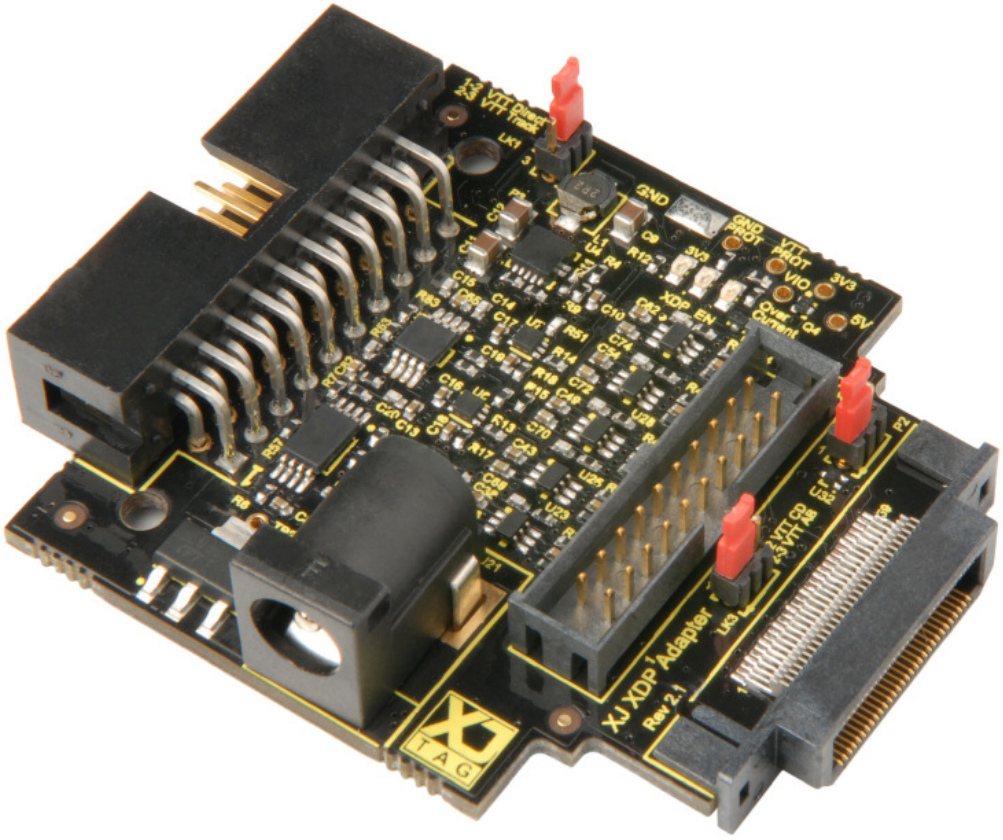
XJTAG® XJXDP

Low Voltage Boundary Scan

User Guide

Version 1.1



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1. Introduction

The XJXDP system complements the XJLink2 by providing a very low impedance drive capability, down to 25 Ω or less. The XJXDP is designed to fit between an XJLink2 and the target Unit Under Test (UUT). Connection between the XJLink2 and XJXDP is via a standard 20-way 0.1" IDC cable. The small form factor board can be directly mounted onto an Intel XDP debug port for minimum wire lengths and maximum performance or it can be connected via a 2 mm ribbon cable for flexibility.

The adapter can normally be powered directly from the XJLink2 via pin1 at 3.3 V but if more power is needed, a power jack can accept external power from 5 V to 15 V.

The XJXDP converts JTAG port signals between the XJLink2 voltage domain (set to 3.3 V) and a UUT low voltage domain (from 3.2 V down to 0.6 V). The XJXDP interface voltage is set by tracking a VTT reference input supplied from the UUT. The XJXDP outputs have the low output impedance required to drive low value termination resistors down to 25 Ω.

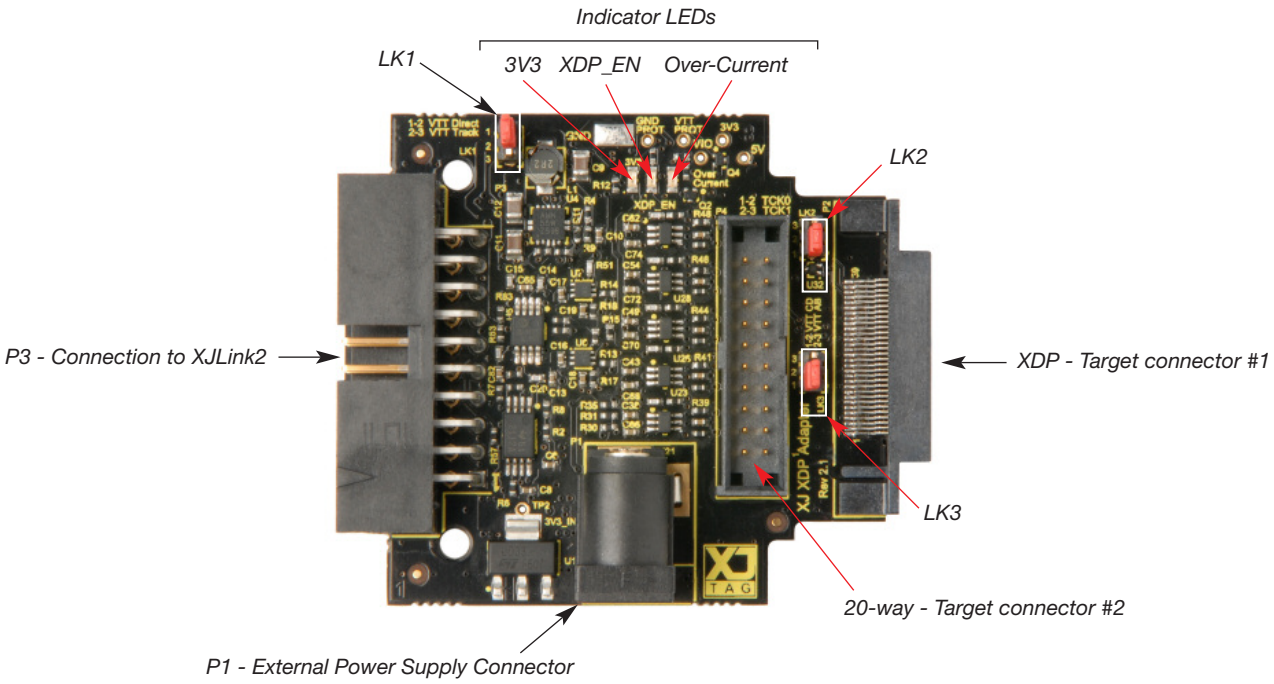


Figure 1 – XJXDP position of connectors, links and indicators

2. Features

- Converts JTAG port signals between 3.3 V domain and low voltage domain down to 0.6 V
- Can drive pull-up or pull-down terminators down to 25 Ω
- Connects to the XJLink2 via a standard 20-way ribbon cable
- Level-translates 8 signals as 5 downlink (XJLink2 to UUT) and 3 uplink (UUT to XJLink2)
- Connects to UUT via the choice of Intel® XDP connector or 20-way 2 mm pitch connector
- Can be powered directly from XJLink2
- Power jack accepts 5 V to 15 V external power when needed
- Over-current trip protects low impedance output drivers from damage when accidentally shorted
- LED indicators show power and trip status
- Can source or sink up to 250 mA to/from UUT termination
- Output impedance <2 Ω at 1 V
- Rise/fall time moderated to between 1.5 ns (50 Ω load) and 3 ns (25 Ω) for low overshoot
- Up to 100 MHz operation
- ESD protection

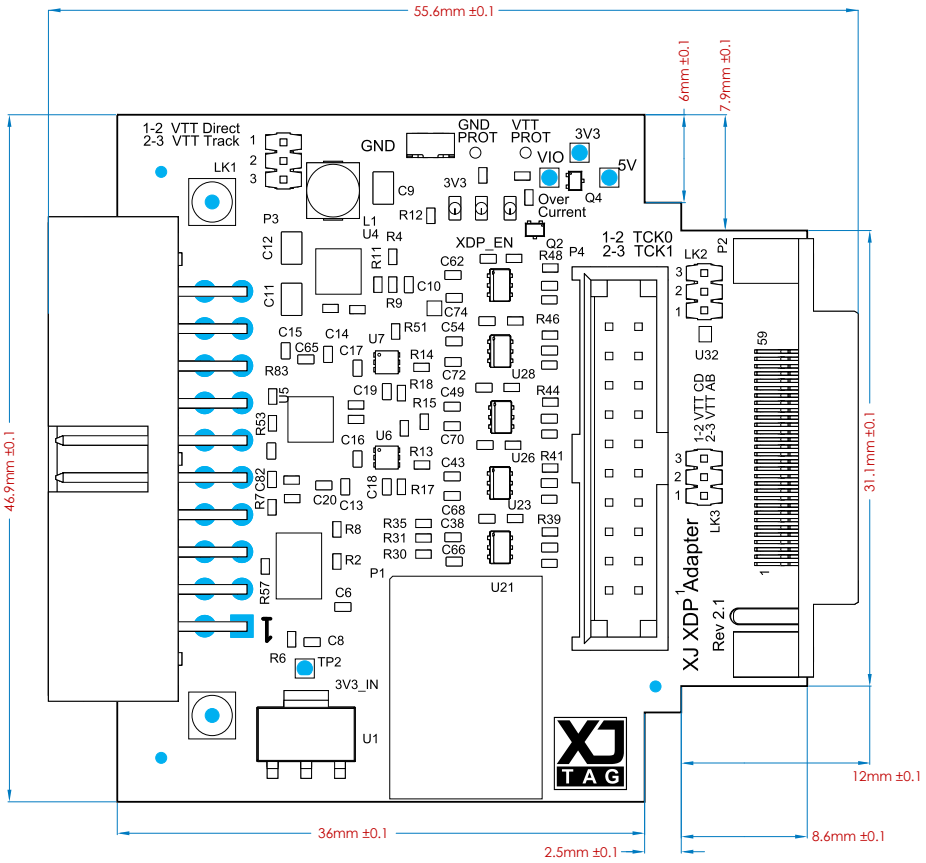


Figure 2 – Dimensions

3. Specifications

Outer dimensions (including connectors)	56 mm length x 47 mm width x 15 mm height
Maximum TCK frequency	100 MHz (depending on cabling and impedance)
XJLink2 signaling and pin 1 power output voltage setting	3.3 V
JTAG voltage with VVT reference tracking regulator	0.6 to 3.2 V
JTAG voltage with external VVT power	0.3 to 3.3 V
Output Rise/fall time (VTT from 0.6 to 2.5V)	1 ns unloaded, 2 ns @ 50 Ω, 3 ns @ 25 Ω
External power (if needed). Connector P1	5 V to 15 V
Quiescent supply current	20 mA
VTT loading	10 kΩ to GND
Output drive impedance	<2 Ω @ 1 V
Maximum combined total output source current before trip	250 mA
Maximum combined total output sink current before trip	250 mA
Input receiver threshold	VTT/2
Input receiver hysteresis	50 mV
Input receiver current loading	<2 µA
XJLink2 connector (P3)	20 pin, dual row, 2.54 mm pitch
Target connector #1 (P4)	20 pin, dual row, 2 mm pitch
Target connector #2 (P2)	Intel XDP connector – Samtec BTH-030-01-L-D-EM2
LK1/2/3	1.27 mm pin header (suitable jumper Harwin M50-2020005)

4. Connector Pin Assignments

Connector P3

(20-way, 2.54 mm pitch, XJLink2 connection)

Pin	Signal Name	I/O	Logic Level	Description
1	VCC	IN	3.3V	Power in / Adapter nRESET
2	GND			Ground
3	TARGET_PGD	OUT	3.3V	Target Power Good (Output from P3)
4	GND			Ground
5	TDI	IN	3.3V	Test Data In (Input to P3)
6	GND			Ground
7	XJL_TMS	IN	3.3V	Test Mode Select (Input to P3)
8	GND			Ground
9	XJL_TCK	IN	3.3V	Test Clock (Input to P3)
10	GND			Ground
11	XJL_RST_OUT#	OUT	3.3V	Target Reset Out (Output from P3)
12	GND			Ground
13	XJL_TDO	OUT	3.3V	Test Data Out (Output from P3)
14	GND			Ground
15	XJL_nTRST	IN	3.3V	Test Reset (Input to P3)
16	GND			Ground
17	XJL_RST_IN#	IN	3.3V	Target Reset In (Input to P3)
18	GND			Ground
19	NO_CONNECT			No connect
20	GND			Ground

Connector P4

(20-way, 2 mm pitch, UUT connector #2)

Pin	Signal Name	I/O	Logic Level	Description
1	VTT	IN		Target Voltage Reference
2	GND			Ground
3	XDP_TARG_PGD	IN	VTT	Target Power Good (Input to P4)
4	GND			Ground
5	XDP_TDI	OUT	VTT	Test Data In (Output from P4)
6	GND			Ground
7	XDP_TMS	OUT	VTT	Test Mode Select (Output from P4)
8	GND			Ground
9	XDP_TCK	OUT	VTT	Test Clock (Output from P4)
10	GND			Ground
11	XDP_RST_OUT#	IN	VTT	Target Reset Out (Input to P4)
12	GND			Ground
13	XDP_TDO	IN	VTT	Test Data Out (Input to P4)
14	GND			Ground
15	XDP_nTRST	OUT	VTT	Test Reset (Output from P4)
16	GND			Ground
17	XDP_RST_IN#	OUT	VTT	Target Reset In (Output from P4)
18	GND			Ground
19	XDP_TCK			Test Clock (optional connection)* (Output from P4)
20	GND			Ground

* Fitting R56 allows XDP_TCK to be driven on two separate pins for low overall cable impedance.

Connector P2

(XDP connector, UUT connector #1)

Pin	Signal Name	I/O	Logic Swing	Description
1	GND			Ground
2	GND			Ground
3	NO_CONNECT			Unused
4	NO_CONNECT			Unused
5	NO_CONNECT			Unused
6	NO_CONNECT			Unused
7	GND			Ground
8	GND			Ground
9	NO_CONNECT			Unused
10	NO_CONNECT			Unused
11	NO_CONNECT			Unused
12	NO_CONNECT			Unused
13	GND			Ground
14	GND			Ground
15	NO_CONNECT			Unused
16	NO_CONNECT			Unused
17	NO_CONNECT			Unused
18	NO_CONNECT			Unused
19	GND			Ground
20	GND			Ground

Pin	Signal Name	I/O	Logic Swing	Description
21	NO_CONNECT			Unused
22	NO_CONNECT			Unused
23	NO_CONNECT			Unused
24	NO_CONNECT			Unused
25	GND			Ground
26	GND			Ground
27	NO_CONNECT			Unused
28	NO_CONNECT			Unused
29	NO_CONNECT			Unused
30	NO_CONNECT			Unused
31	GND			Ground
32	GND			Ground
33	NO_CONNECT			Unused
34	NO_CONNECT			Unused
35	NO_CONNECT			Unused
36	NO_CONNECT			Unused
37	GND			Ground
38	GND			Ground
39	XDP_TARG_PGD	IN	VTT	Target Power Good (Input to P2)
40	NO_CONNECT			
41	NO_CONNECT			
42	NO_CONNECT			
43	VTT	IN		Target Voltage Reference (Input to P2)
44	NO_CONNECT			
45	NO_CONNECT			Unused
46	NO_CONNECT			Unused
47	NO_CONNECT			Unused
48	NO_CONNECT			Unused
49	GND			Ground
50	GND			Ground
51	NO_CONNECT			Unused
52	XDP_TDO	IN	VTT	Test Data Out (Input to P2)
53	NO_CONNECT			Unused
54	XDP_nTRST	OUT	VTT	Test Reset (Output from P2)
55	XDP_TCK1	OUT	VTT	Test Clock #1 (Output from P2)
56	XDP_TDI	OUT	VTT	Test Data In (Output from P2)
57	XDP_TCK0	OUT	VTT	Test Clock #0 (Output from P2)
58	XDP_TMS	OUT	VTT	Test Mode Select (Output from P2)
59	GND			Ground
60	XDP_PRESENT_N	OUT	VTT	Test system present when low (Output from P2)

5. Operating Instructions

Quick start instructions

1 Connect the XJXDP to the XJLink2 using a 20-way ribbon cable
2 Set XJLink bank voltage to 3.3 V
3 Enable power on XJLink2 pin 1
4 3V3 LED lights when board power is present
5 XDP_EN LED lights when XJLink2 pin1 is powered, all power rails are good and VTT is tracking a valid VTT voltage 0.6 V < VTT < 3.2 V
6 If an output is shorted or is over-current, the adapter will trip, causing the red 'Over-Current' LED to light
7 To reset the trip, you must cycle the power to XJLink2 pin1
8 If either of the green LEDs dims during use or operation is unreliable, supply external power via the power jack

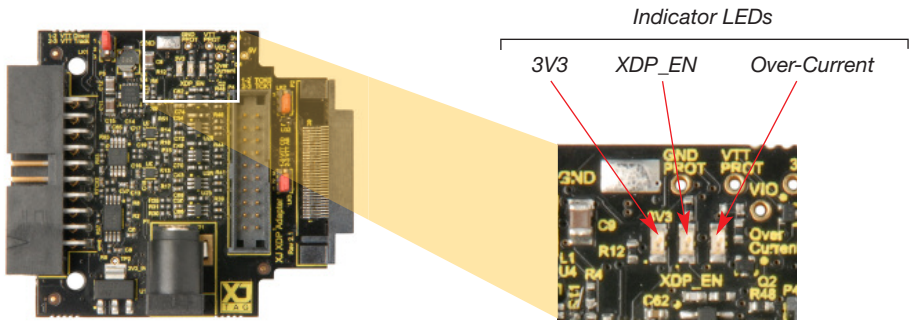


Figure 3

Detailed description

The XJXDP converts JTAG port signals between the XJLink2 voltage domain (set to 3.3 V) and a UUT interface voltage, set by the VVT input. The XJXDP logic output level tracks the VTT reference input supplied by the UUT. The XJXDP outputs have the low output impedance required to drive low value termination resistors down to 25 Ω.

The XJXDP tracks VTT reference voltages between 0.6 V and 3.2 V. Comparator circuits check that the tracking regulator is correctly tracking the VTT reference to within +/- 5%. If the tracking regulator falls outside of this tolerance band, then the XDP output drivers will be disabled and the green XDP_EN indicator LED will be turned off (see Table 1).

The XJXDP connects to the XJLink2 via a standard 20-way ribbon cable. For the highest clock speeds, the ribbon cable should be kept as short as possible. Figure 4 shows an example Pin Mapping. The pins on P2 and P4 are high impedance until power is provided to pin 1 of P3. Once power is applied the I/O pins on the XJXDP become active. Pin 1 on the XJLink must always be high to enable the XJXDP even when powering the XJXDP from an external source.

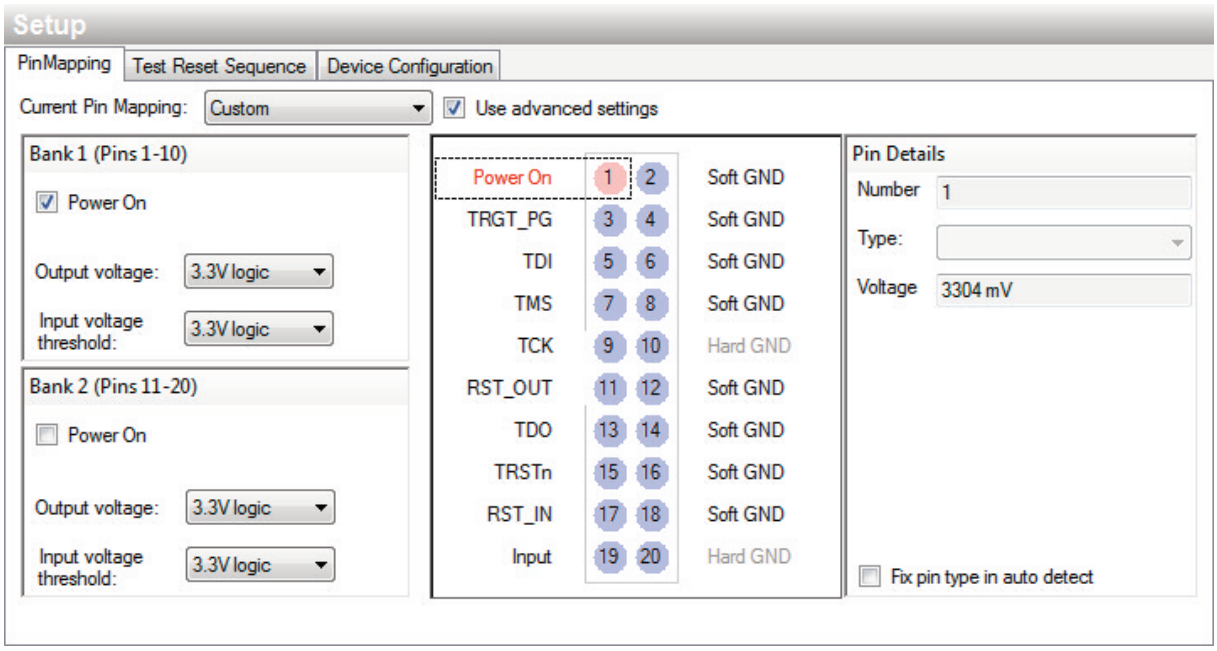


Figure 4 – Example Pin Map for default configuration

The XJXDP is designed to drive cables with very low value terminating resistors, down to 25 Ω. This means that the output drivers must have very low 'on' resistance, typically 2 Ω. Consequently, any short circuit of the output pins would cause a large output current that could risk damaging the driver devices. To guard against this, both the GND and VTT rails supplying the drivers include a current sensing trip that disables the output drivers if the combined source or sink current exceeds 250 mA. If the trip condition is activated the RED Over-Current LED will light (see Table 1). The trip condition can be reset by cycling the pin1 power from the XJLink2.

LED	Colour	Meaning when 'ON'
3V3	Green	XJXDP is receiving XJLink2 or external power.
XDP_EN	Green	Internal power rails and VTT tracking are within limits and XDP drivers are enabled
Over_Current	Red	Indicates trip condition when total output source or sink current exceeds 250 mA

Table 1

The XJXDP has two UUT connection options. P2 is an Intel XDP compatible connector which is designed to be plugged directly onto the target board for minimum connection length and maximum TCK frequency. The Intel® XDP connector allows for two TCK signals: TCK0 on P2 pin 57 and TCK1 on P2 pin 55, with TCK0 being the default. The XJXDP can be configured to drive either clock signal by fitting the LK2 jumper in the desired position (see table 2). Though the jumper does not physically allow driving both TCK0 and TCK1, the XJXDP does have the output drive strength to simultaneously drive both TCK0 and TCK1 at 50 Ω termination so, if required, both connections could be made.

Link	Link fitted connecting pin1 - pin2	Link fitted connecting pin2 - pin3
LK1	Take power directly from UUT VTT	Select tracking regulator
LK2	Drive TCK onto P2, pin 57, TCK0	Drive TCK onto P2, pin 55, TCK1
LK3	Take tracking reference from P2, pin 44, VTT_CD	Take tracking reference from P2, pin 43, VTT_AB

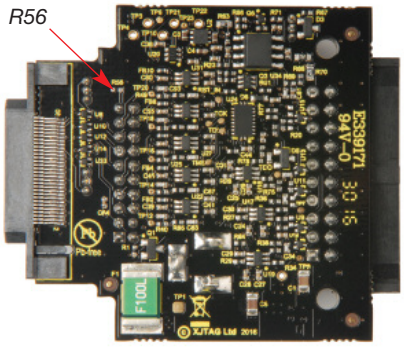
Table 2

Similarly, the Intel® XDP connector (P2) provides the VTT reference voltage on one of two pins: VTT_AB on pin 43 and VTT_CD on pin 44, with VTT_AB being the default. Which of these two is used as the reference for the XJXDP tracking power supply can be selected using LK3 (see Table 2).
(Note that P4 pin 1 is always available as the VTT reference input regardless of the setting of LK3)

For applications where the UUT does not have an Intel XDP connector, an alternative 20-way, 2 mm pitch connector P4 can be used to connect to a UUT via a ribbon cable. Since a ribbon cable has high characteristic impedance compared to the 50 Ω or 25 Ω termination resistance typically used on the UUT, there will inevitably be some termination mismatch. The effects of any mismatch on signal integrity can be minimized by keeping the cabling as short as possible. The most critical signal in any JTAG interface is the TCK signal. In order to be able to lower the characteristic impedance of the TCK signal, the TCK driver can drive P4 pins 9 and 19 in parallel to give a lower combined impedance by soldering a 0 Ω link in position R56.

For good performance, it is important to adhere to the following guidelines:

- Keep the 2 mm ribbon cable assembly as short as possible
- Connect all of the even numbered pins (GND connections) to the signal ground of the UUT



6. Powering the XJXDP

The XJXDP is designed to be powered directly from the XJLink2. Normally this provides sufficient power, since the XJXDP uses a high efficiency switching converter to generate an internal VTT supply that tracks the VTT reference input. At VTT = 1 V, nearly 250 mA of output current is available from the tracking supply without external power. Note that signals that are terminated with a pull-up on the UUT do not draw from this output current budget, because the terminator current is supplied by the UUT VTT rail. Only pull-down terminations on the UUT require power from the XJXDP adapter.

When powered from the XJLink2, the XJXDP includes a current limit on the 3.3 V input from the XJLink2, to prevent excessive current from being drawn. If either of the green LEDs dims or flickers or the scan-chain breaks sporadically, the user should try supplying external power (see below) as a first step, before looking for other causes.

For the case where the available current from the XJLink2 is insufficient, a power jack is provided to accept external power from a mains power adapter outputting 5 V to 15 V. The external power is regulated down to 3.3 V via a linear regulator, so when outputting large amounts of current on the output pins it is strongly advised to use an adapter at the lower end of the range (less than 6 V, ideally) to avoid high power dissipation. If higher external voltage is combined with high output current, be aware that some parts of the adapter can become hot.

The tracking regulator enables a very low loading on the VTT reference supplied from the UUT. Using the tracking regulator imposes the lower voltage limit of 0.6 V. If the output logic level is required to be between 0.6 V and 0.3 V then LK1 can be used to take power directly from the UUT VTT reference output (see Table 2). Many UUTs have plenty of power available from the VTT reference output.
NOTE: Even when not using pin 1 on the XJLink to power the XJXDP board it needs to be set high to enable the board.