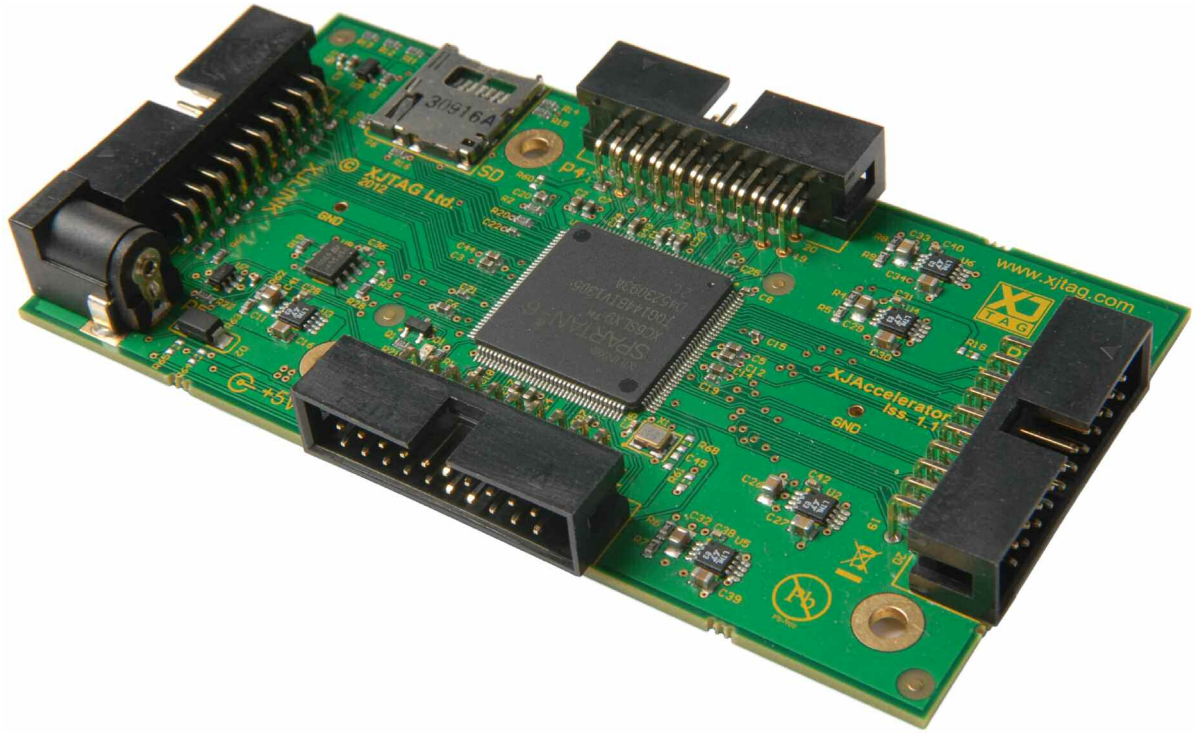
XJTAG®

XJAccelerator v1

User Guide

Version 1



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1. Introduction

The XJAccelerator is a configurable FPGA board with three I/O connectors that can run on different voltage domains. The board's main uses are:

- high-speed programming of flash memories when a PCB doesn't have a suitable FPGA for accelerated programming.
- high-speed programming of multiple devices concurrently, including when they are different device types with different interfaces.
- to act as a JTAG Multiplexer (scan bridge).
- to act as a mini I/O expander.

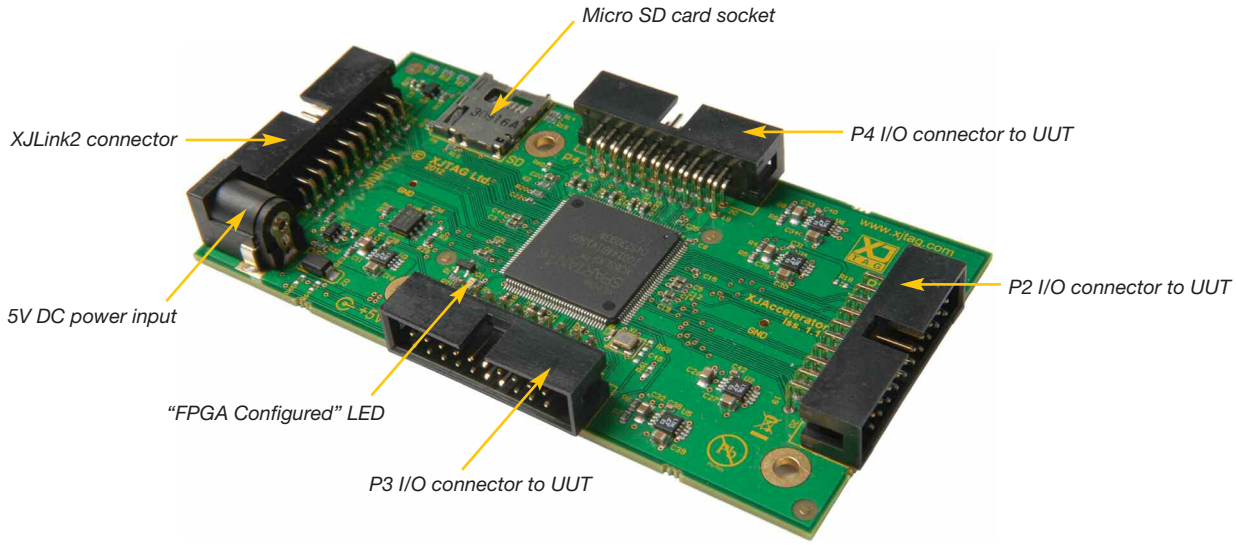

Figure 1 – XJAccelerator Board

The board's interfaces are:

1. XJLink2 connector
2. 5V DC power input
3. Micro SD card socket
4. "FPGA Configured" LED
5. P2 I/O connector to UUT
6. P3 I/O connector to UUT
7. P4 I/O connector to UUT

When used for accelerated programming, the data can be streamed to the FPGA using JTAG, or retrieved from a micro SD card. The I/O connectors provide the interfaces to the devices to be programmed.

When used as a JTAG multiplexer, the UUT's JTAG chains are connected to the XJAccelerator's I/O connectors, and the TDO Switch should be set so that the XJLink2 receives JTAG data from the FPGA's logic instead of its JTAG port (see *Routing TDO* on page 8).

2. XJAccelerator Block Diagram

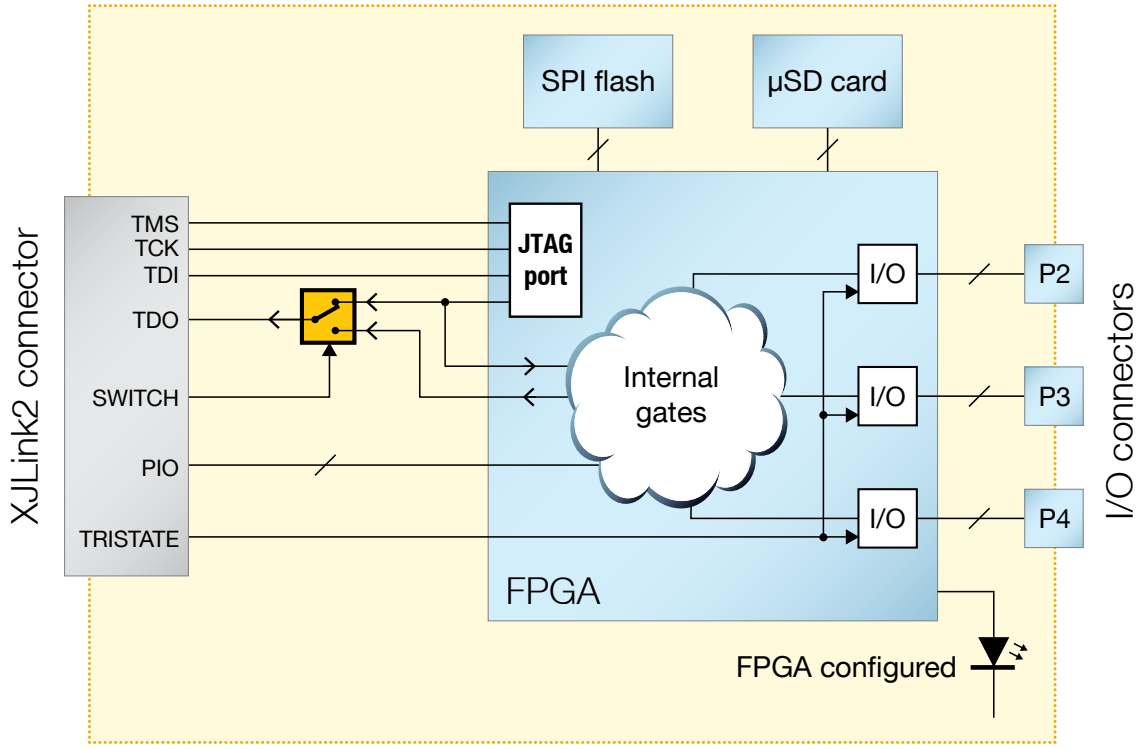

Figure 2 – XJAccelerator Block Diagram

3. Powering the XJAccelerator

The board is powered from a DC input socket.

Connector type: 2.1 mm central pin, 5.5 mm outer diameter, 9.5 mm barrel length.
Suitable mating plug: Farnell 224923, Digi-Key EP501A-ND, RS 487-858.

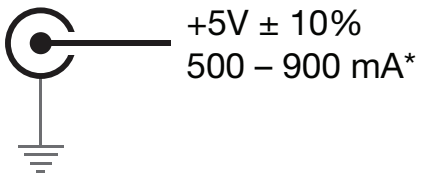

Figure 3 – DC Power Input

* 500 mA is suitable for most setups. However, the current requirement may exceed this depending on output loading and how the FPGA is configured.

4. XJLink2 Connector Pinout (P1)

The XJLink2 connects to the board using P1. The JTAG interface and this connector's PIO operate at 3.3 V, which cannot be changed. The pinout is shown in Table 1.

Pin	Signal	Function
1	TRISTATE	High: puts FPGA I/O into tristate mode. (PCB has a 4k7 pulldown)
2	SWITCH	Low: TDO comes from the FPGA's JTAG port only High: TDO comes from the FPGA's internal logic
3	TDO	From either the FPGA's JTAG port or the FPGA's internal logic depending on state of signal SWITCH
4	PIO 4	PIO connected to FPGA bank 2 pin 66
5	TDI	JTAG TDI signal from the XJLink2
6	PIO 6	PIO connected to FPGA bank 2 pin 62
7	TMS	JTAG TMS signal from the XJLink2
8	PIO 8	PIO connected to FPGA bank 2 pin 61
9	TCK	JTAG TCK signal from the XJLink2
10	GND	
11	PIO 11	PIO connected to FPGA bank 2 pin 59
12	PIO 12	PIO connected to FPGA bank 2 pin 58
13	PIO 13	PIO connected to FPGA bank 2 pin 57
14	PIO 14	PIO connected to FPGA bank 2 pin 56
15	PIO 15	PIO connected to FPGA bank 2 pin 55
16	PIO 16	PIO connected to FPGA bank 2 pin 51
17	PIO 17	PIO connected to FPGA bank 2 pin 50
18	PIO 18	PIO connected to FPGA bank 2 pin 48
19	PIO 19	PIO connected to FPGA bank 2 pin 47
20	GND	

Table 1 – XJLink2 Input Connector Pinout

Connector type: keyed 20-pin 0.1" pitch.
Suitable mating connector: Farnell 1200505, Digi-Key 1195-7010-ND, RS 426-3766.

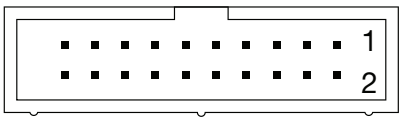

Figure 4 – XJLink2 Connector

5. I/O Connectors

The board has three I/O connectors, P2 – P4, that connect to PIO on the FPGA.
Pins 10 and 20 are connected to ground.
Connector type: keyed 20-pin 0.1" pitch.
Suitable mating connector: Farnell 1200505, Digi-Key 1195-7010-ND, RS 426-3766.

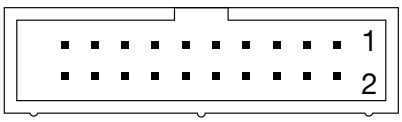

Figure 5 – I/O Connector

6. I/O Pinout

Connector Pin	FPGA Pin (bank 0)	Connector Pin	FPGA Pin (bank 0)
1	143	2	142
3	141	4	111
5	138	6	117
7	134	8	118
9	127	10	GND
11	119	12	123
13	124	14	126
15	132	16	133
17	137	18	139
19	140	20	GND

Table 2 – P2 I/O Pinout

Connector Pin	FPGA Pin (bank 1)	Connector Pin	FPGA Pin (bank 1)
1	104	2	102
3	101	4	100
5	99	6	98
7	97	8	94
9	93	10	GND
11	88	12	92
13	85	14	87
15	83	16	84
17	81	18	82
19	80	20	GND

Table 3 – P3 I/O Pinout

Connector Pin	FPGA Pin (bank 3)	Connector Pin	FPGA Pin (bank 3)
1	35	2	34
3	33	4	32
5	30	6	29
7	26	8	24
9	23	10	GND
11	12	12	14
13	10	14	11
15	6	16	7
17	2	18	5
19	1	20	GND

Table 4 – P4 I/O Pinout

7. I/O Voltage Domains

The three I/O connectors can be configured for different voltages to match the I/O standard selected for FPGA banks 0, 1, and 3 when the device was configured. The voltages provided by the hardware are adjusted by changing the resistors shown in Table 5. Table 6 lists the values required for standard I/O voltages, and Figure 6 shows the location of these resistors on the PCB.

The factory-built setting for every bank is 3V3.

I/O Connector	Resistor
P2 (FPGA bank 0)	R4
P3 (FPGA bank 1)	R6
P4 (FPGA bank 3)	R8

Table 5 – Resistors to Configure the I/O Voltage Domains

I/O Voltage	Value
3V3	86K6 ±1% 0603 0.0625W
2V5	53K6 ±1% 0603 0.0625W
1V8	24K3 ±1% 0603 0.0625W
1V5	11K5 ±1% 0603 0.0625W

Table 6 – Resistor Values to Configure the I/O Voltage Domain

Note: the recommended operating voltage range for the I/O domains is 1.1 – 3.45 V.
Care must be taken when changing these resistors to ensure voltages are maintained within that range.

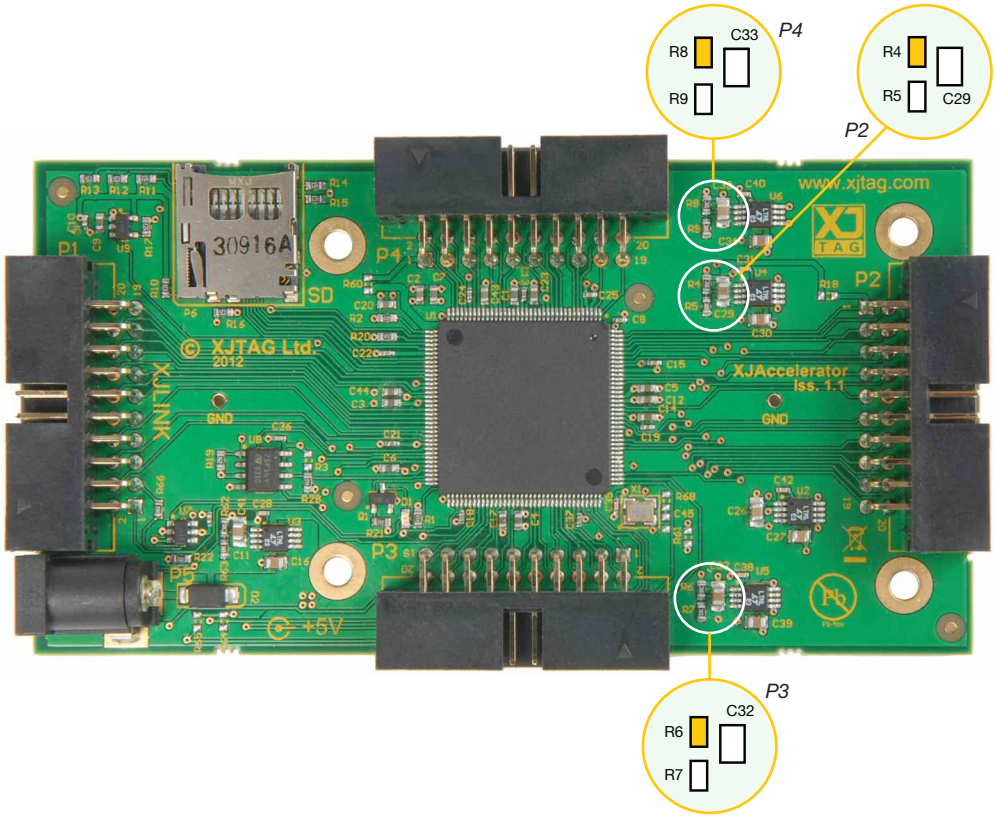

Figure 6 – Locating the Resistors to Configure I/O Voltages

8. I/O Electrical Characteristics

The characteristics of the signals on the three I/O connectors will be determined by how the FPGA has been configured. However, it is normal to use the LVCMOS standards for the I/O, in which case the logic thresholds will be as listed in Table 7 (voltages stated are valid across all possible drive strengths). Their values are dependent on the voltage domain that has been selected for that bank of I/O.

Voltage Domain	V_{IL} (min)	V_{IL} (max)	V_{IH} (min)	V_{IH} (max)	V_{OL} (max)	V_{OH} (min)
3V3	-0.5	0.80	2.0	4.1	0.40	2.90
2V5	-0.5	0.70	1.7	4.1	0.40	2.10
1V8	-0.5	0.38	0.8	4.1	0.45	1.35
1V5	-0.5	0.38	0.8	4.1	0.38	1.13

Table 7 – I/O Logic Thresholds (LVCMOS standards)

The maximum current capability of the pins is dependent on the drive strength set when the FPGA was configured. Possible options are listed in Table 8; they are dependent on the I/O interface voltage and the connector being used.

Voltage Domain	P2 (mA)	P3 (mA)	P4 (mA)
3V3	2, 4, 6, 8, 12, 16, 24	2, 4, 6, 8, 12, 16, 24	2, 4, 6, 8, 12, 16, 24
2V5	2, 4, 6, 8, 12, 16	2, 4, 6, 8, 12, 16, 24	2, 4, 6, 8, 12, 16, 24
1V8	2, 4, 6, 8, 12, 16	2, 4, 6, 8, 12, 16, 24	2, 4, 6, 8, 12, 16, 24
1V5	2, 4, 6, 8	2, 4, 6, 8, 12, 16	2, 4, 6, 8, 12, 16

Table 8 – FPGA Drive Strength Options

9. Setting the I/O into a Tristate Condition

The FPGA's I/O can be placed into a tristate condition using the TRISTATE signal on the XJLink2 connector (pin 1) provided the FPGA has been configured and its image has been designed to support this feature. The board has a 4k7 pulldown on the TRISTATE control input.

TRISTATE (pin 1)	I/O Pins' condition
Low	Normal use
High (+3V3)	Tristate mode

Table 9 – Placing the I/O into a Tristate Mode

10. Routing TDO

The TDO signal can be returned to the XJLink2 either directly from the FPGA's JTAG port (e.g. when using the XJAccelerator for programming) or from the FPGA's internal logic (e.g. when using it as a JTAG multiplexer) as shown in Figure 7.

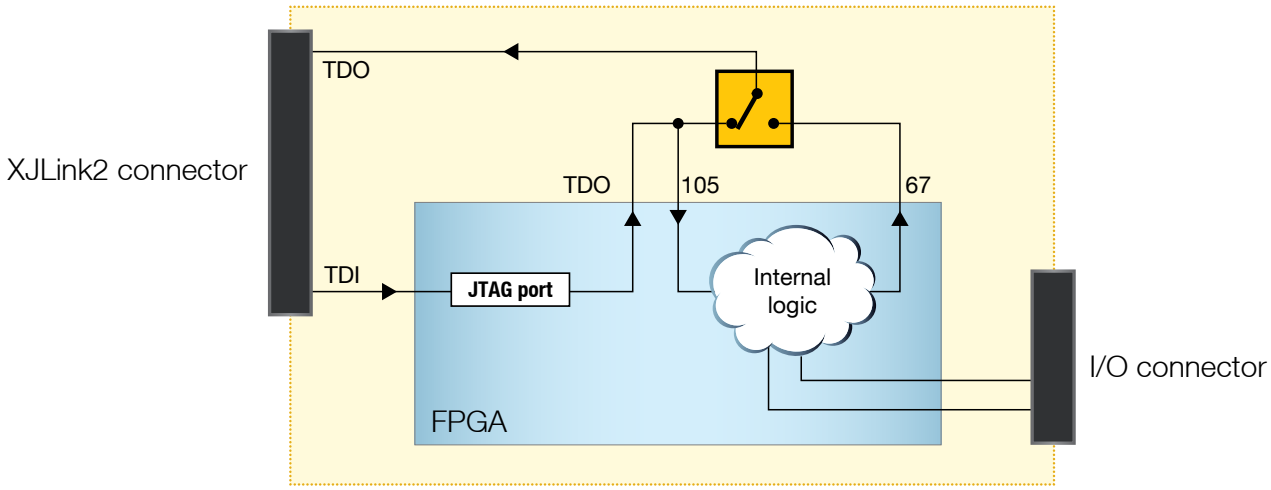

Figure 7 – TDO Routing

The TDO source is determined by the state of the SWITCH signal on the XJLink2 connector as described in Table 10.

SWITCH (pin 2)	TDO source
Low	FPGA's JTAG port
High (+3V3)	FPGA's internal logic

Table 10 – Selecting the Source of TDO

11. Passthrough Mode

The XJAccelerator can be configured in hardware so that some of the signals to/from the XJLink2 are routed directly to connectors P2 and P3. This can be used, for example, to utilise the XJLink2's frequency or analogue voltage measuring capabilities. Table 11 lists the locations where 0603 0 Ω links need to be placed.

Note: voltages applied in passthrough mode must not exceed the limits set by the FPGA because the signals are still applied to the FPGA in this mode (see the *Voltage Domains* section on page 7).

To avoid the FPGA attempting to drive nets that are being used as passthrough, a suitable FPGA image should be used, or Disable Values or Constant pins should be set in the project.

XJLink Pin	P2 Pin	P2 Link	P3 Pin	P3 Link
4	4	R29	4	R41
6	6	R30	6	R42
8	8	R31	8	R43
11	11	R23	11	R36
12	12	R32	12	R44
13	13	R24	13	R37
14	14	R33	14	R45
15	15	R25	15	R38
16	16	R34	16	R46
17	17	R26	17	R39
18	18	R35	18	R47
19	19	R27	19	R40

Table 11 – Hardware Configuration to Route Directly to the XJLink2

The links are located on the underside of the board at the positions shown in Figure 8.

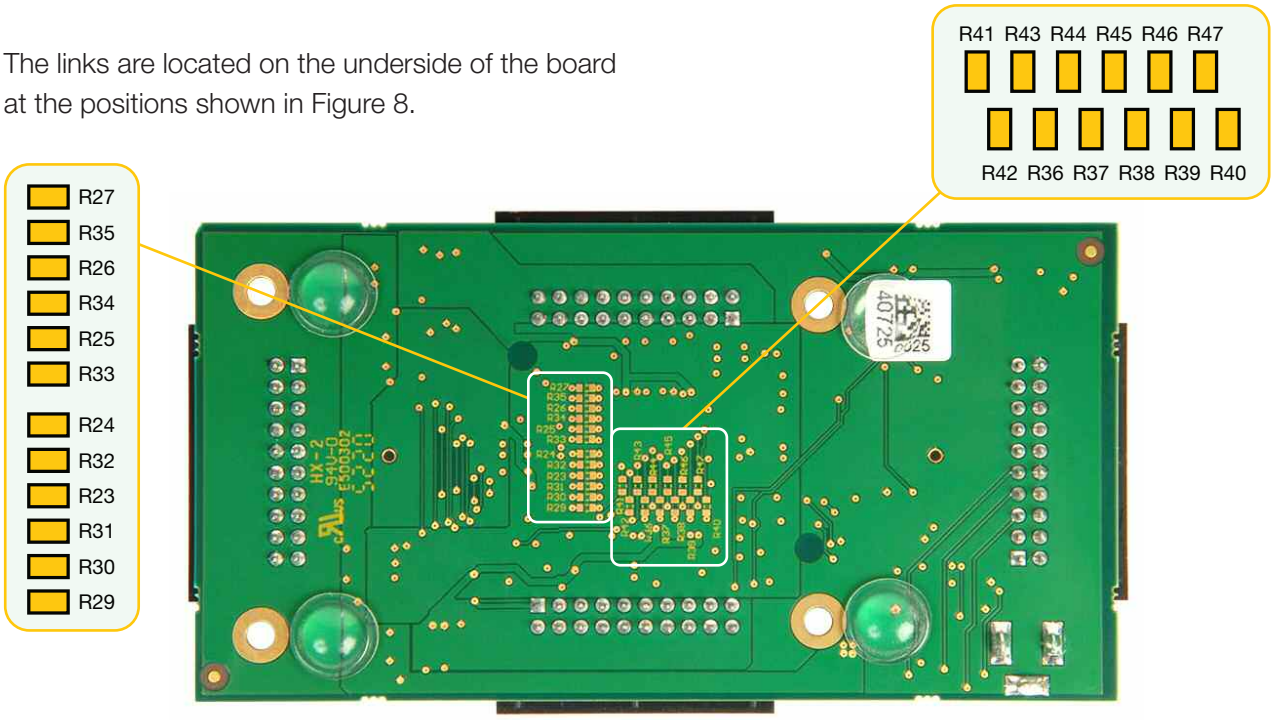

Figure 8 – Locating the Links to Configure Passthrough Mode

12. Programming FPGA Images

The XJAccelerator uses a Xilinx® Spartan®-6 SLX9 FPGA in a 144-pin footprint. It can be programmed over the JTAG interface or from the on-board SPI flash memory.

The board's LED indicates that the FPGA has been configured. When the image is stored in the on-board flash memory, the LED should illuminate shortly after power-up; if the board is unprogrammed, the LED will remain off.

It is advisable to write the associated XJEase tests so that it automatically commences programming if an unconfigured FPGA is detected (NB: when used as a mini I/O board, no programming is needed). When written in this way, it is helpful if the code implements the following sequence:

1. Confirm the XJAccelerator FPGA is accessible via JTAG.
2. Check if the FPGA has been configured from the correct image.
3. If the FPGA is unprogrammed or does not contain the expected image, automatically program the on-board flash with the required image and then force the FPGA to reload from it.

XJTAG can supply the XJAccelerator together with an XJDeveloper board file and the associated XJEase files to provide this functionality.

13. µSD Card Socket

A micro-SD card socket is provided for additional storage. When using the XJAccelerator for programming, it can be used to store the data to be programmed as an alternative to streaming it to the board over JTAG.