XJTAG®

XJAccelerator SODIMM Module Hardware

User Guide

Version 1

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1. Introduction

The XJAccelerator SODIMM module is a multi-purpose FPGA board in a 260-pin SODIMM form factor that is designed to be integrated into a test fixture assembly to simplify fixture design and reduce development time. Its main applications are to:

- extend test coverage by providing additional connectivity.
- act as a JTAG multiplexer (scan bridge).
- act as a mini I/O expander.
- facilitate high-speed accelerated programming of flash memories.
- add a high-speed digital bus to the test system

Each of the FPGA's four voltage banks can be powered independently to provide versatile I/O interface levels.

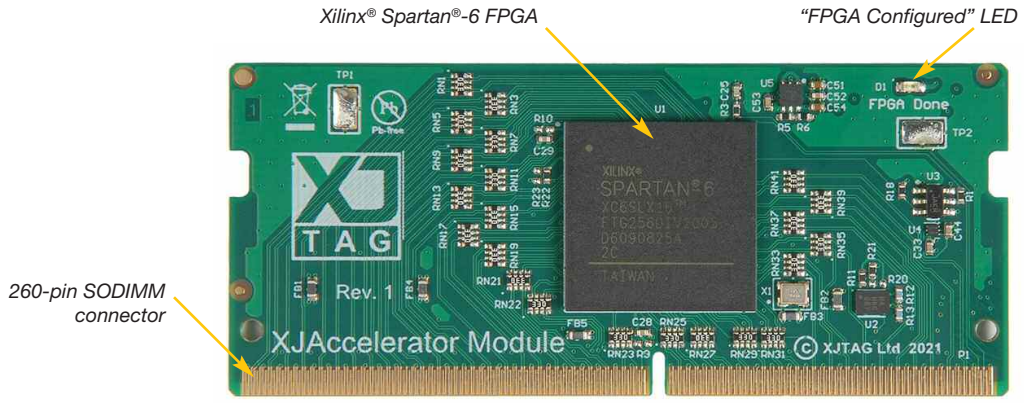

Figure 1 – XJAccelerator SODIMM Module

2. Description & Block Diagram

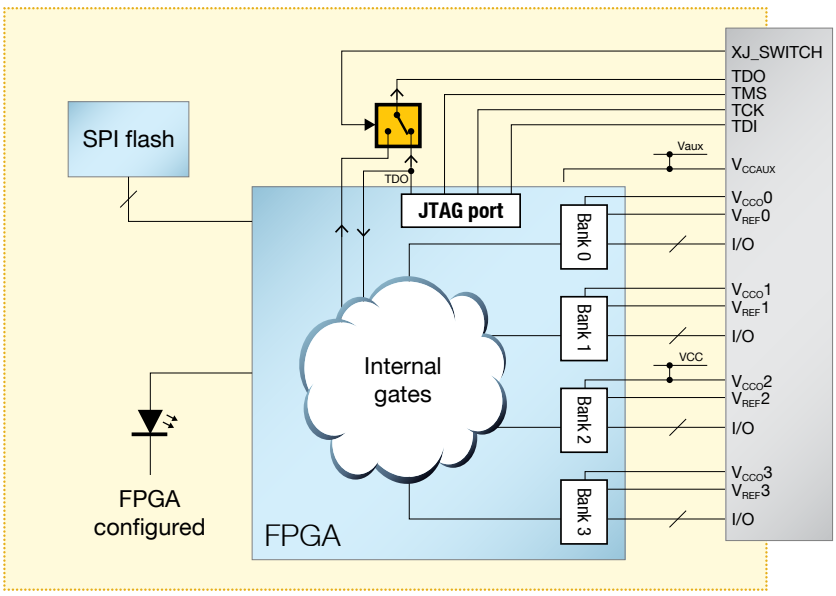

Figure 2 – Block Diagram

The module provides up to 163 single-ended I/O, divided between the four voltage banks. Most of these I/O can be configured to provide balanced pairs; in total, up to 79 differential pairs are available. Each voltage bank has a separate supply to allow up to 4 different I/O voltages to be used.

The JTAG interface is powered from the FPGA's Aux supply to allow it to be operated at voltages that are independent of the I/O voltage domains. The TDO signal can be routed to the connector either directly from the FPGA's TAP or via the FPGA's internal logic; the latter provides the option of using the module as a JTAG multiplexer. This routing is controlled by the XJ_SWITCH signal.

An on-module flash is provided to hold the FPGA's firmware. The module has an LED that is driven from the FPGA to provide an indication that the FPGA is configured.

3. Powering the XJAccelerator SODIMM Module

The board is powered from pins on the SODIMM connector. Each of the FPGA's voltage banks are separately connected to allow them to operate at different voltages.
V_{CCAUX} and the Bank 2 supply also power circuitry on the module.

Module Pin	Description	Min	Typ	Max	Units
7, 8, 25, 26, 43, 44	Bank 0 supply	1.1		3.45	V
205, 206, 223, 224, 241, 242	Bank 1 supply	1.1		3.45	V
157, 158, 175, 176, 187, 188	Bank 2 supply[1]	1.65		3.45	V
61, 62, 79, 80, 97, 98	Bank 3 supply	1.1		3.45	V
109, 110, 121, 122, 133, 134	V_{CCAUX}[2][3]	2.375	2.5	2.625	V
1, 2, 13, 14, 19, 20, 31, 32, 37, 38, 49, 50, 55, 56, 67, 68, 73, 74, 85, 86, 91, 92, 103, 104, 115, 116, 127, 128, 139, 140, 145, 146, 151, 152, 163, 164, 169, 170, 181, 182, 193, 194, 199, 200, 211, 212, 217, 218, 229, 230, 235, 236, 247, 248, 253, 254, 259, 260	GND	3.15	3.3	3.45	V

Table 1 – Powering the module

[1] Bank 2 input supply also powers peripherals on the module.
[2] The Aux supply also powers the JTAG interface.
[3] During FPGA configuration, the 2.5 V Aux supply must be used if Bank 2's supply is 1.8 V.

During FPGA configuration, the 2.5 V AUX supply is required if a 1.8 V supply is used for Bank 2's supply. In addition, if you are using a logic standard other than LVCMOS, please refer to the Xilinx datasheets as some FPGA versions may need a 2.5 V AUX supply for other logic standards.

The module's supply current requirements depend on many factors including the loading on I/O pins, the choice of voltage domain, and the speed of I/O transitions. To calculate the expected current for each supply rail, refer to the Xilinx Spartan 6 datasheets.

The Xilinx FPGA's V_{CCINT} supply is derived on the module from the V_{CCAUX} input, so this must be included when calculating the total current required for the V_{CCAUX} supply pin.
Note that an additional 20 mA is drawn by the Bank 2 supply voltage V_{CCO2} due to on-module circuitry.

4. JTAG Interface

The JTAG interface is connected to the SODIMM connector as described in Table 2 below. It is powered from the V_{CCAUX} supply, and the required pull resistors and high-speed terminations are fitted on the module so that external pull resistors are not required.

Module Pin	Description	Comments
255	TMS	
256	TDI	
257	TCK	Max 18 MHz
258	TDO	See Figure 3

Table 2 – JTAG Interface Pinout

The TDO signal from the module can either be taken directly from the FPGA's JTAG port or via its internal logic. It is routed by a hardware switch on the module and for most applications (e.g. when the XJAccelerator is providing extra connectivity or being used for accelerated programming), the switch position can be fixed to take TDO from the FPGA's JTAG port. For some applications, such as when the module is used as a JTAG multiplexer, TDO can instead be routed through the FPGA's internal gates as illustrated by the example in Figure 3. The routing of TDO is controlled by the XJ_SWITCH signal from the SODIMM connector.

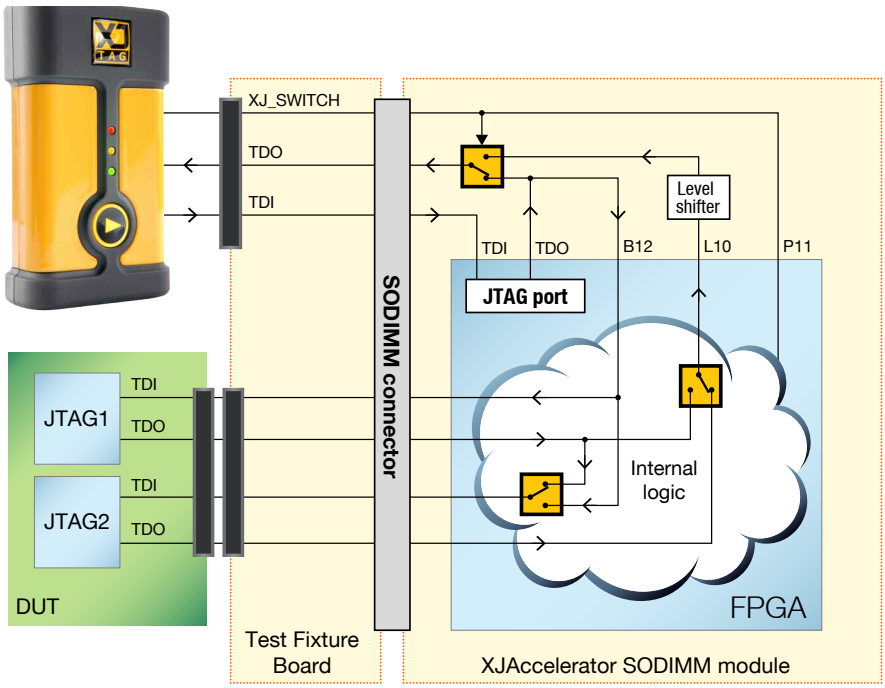

Figure 3 – An Example of TDO Routing For a JTAG Multiplexer

Module Pin	FPGA Pin	XJTAG Net Name	Comment
N/A	B12	FPGA_TDO	Connected to the FPGA JTAG port's TDO
N/A	L10	IO_TDO_A	Connected via a level shifter to an input on the TDO switch
162	P11	XJ_SWITCH	Controls TDO routing (see Table 4)

Table 3 – TDO Switch Pinout

XJ_SWITCH	TDO source	Comment
Low	TDO from the FPGA's JTAG port is routed directly to	
High	TDO passes through the FPGA's internal logic before being routed to the connector's TDO pin.	The logic High level is determined by the V_{CCAUX} voltage

Table 4 – TDO Switch Pinout

When TDO is taken from the FPGA's internal logic, the signal exits the FPGA on a Bank 2 pin. However, a voltage level shifter on the module adjusts the TDO voltage to match that of the other JTAG signals.

5. I/O Connections

Bank	Max available singled-ended I/O[4]
0	35
1	51
2	26
3	51

Table 5 – Available single-ended I/O

[4] Up to a further four additional I/O are available if I/O standards are used that do not require an external VREF to be applied. In that situation, VREF inputs can be used for I/O. However, due to on-board capacitance, they should only be used for slow signals. See Table 11.

Most of those I/O can alternatively be used as differential pairs. The maximum number of differential I/O available in each bank is shown in Table 6. Each bank can have a mix of single-ended I/O and differential pairs.

Bank	Maximum Available I/O
0	17 differential pairs[5] + 1 single-ended
1	25 differential pairs[5] + 1 single-ended
2	12 differential pairs[5] + 2 single-ended
3	25 differential pairs[5] + 1 single-ended

Table 6 – Maximum Available Differential Pair I/O

[5] Each unused differential pair can instead be used as two single-ended I/O

The following tables list the SODIMM connector pins for the FPGA's I/O.

Module Pin	FPGA Pin	XJTAG Net Name
3	A14	B0_0_N
5	B14	B0_0_P
9	A13	B0_2_N
11	C13	B0_2_P
15	A11	B0_4_N
17	C11	B0_4_P
21	A10	B0_6_N
23	B10	B0_6_P
27	A9	B0_8_N
29	C9	B0_8_P
33	A8	B0_10_N
35	B8	B0_10_P
39	A7	B0_12_N
41	C7	B0_12_P
45	A6	B0_14_N
47	B6	B0_14_P
51	A5	B0_16__N
53	B5	B0_16_P

Module Pin	FPGA Pin	XJTAG Net Name
4	D12	B0_1_N
6	D11	B0_1_P
10	E11	B0_3_N
12	F10	B0_3_P
16	C10	B0_5_N
18	E10	B0_5_P
22	D9	B0_7_N
24	F9	B0_7_P
28	D8	B0_9 (single-ended only)
34	E8	B0_11_N
36	E7	B0_11_P
40	C6	B0_13_N
42	D6	B0_13_P
46	C5	B0_15_N
48	D5	B0_15_P
52	E6	B0_17_N
54	F7	B0_17_P

Table 7 – Bank 0 I/O pins

Module Pin	FPGA Pin	XJTAG Net Name
177	T12	B1_0_N
179	R12	B1_0_P
183	T13	B1_2_N
185	T14	B1_2_P
189	T15	B1_4_N
191	R14	B1_4_P
195	R16	B1_6_N
197	R15	B1_6_P
201	P16	B1_8_N
203	P15	B1_8_P
207	N16	B1_10_N
209	N14	B1_10_P
213	M16	B1_12_N
215	M15	B1_12_P
219	L16	B1_14_N
221	L14	B1_14_P
225	K16	B1_16_N
227	K15	B1_16_P
231	J16	B1_18_N
233	J14	B1_18_P
237	H16	B1_20_N
239	H15	B1_20_P
243	G16	B1_22_N
245	G14	B1_22_P
249	F16	B1_24_N
251	F15	B1_24_P

Module Pin	FPGA Pin	XJTAG Net Name
178	K11	B1_1_N
180	K12	B1_1_P
184	M14	B1_3_N
186	M13	B1_3_P
190	J12	B1_5_N
192	J11	B1_5_P
196	K14	B1_7_N
198	J13	B1_7_P
202	H14	B1_9_N
204	H13	B1_9_P
208	H11	B1_11_N
210	G12	B1_11_P
214	G11	B1_13_N
216	F12	B1_13_P
220	F14	B1_15_N
222	F13	B1_15_P
226	E16	B1_17_N
228	E15	B1_17_P
232	D16	B1_19_N
234	D14	B1_19_P
238	C16	B1_21_N
240	C15	B1_21_P
244	B16	B1_23_N
246	B15	B1_23_P
250	E13	B1_25 (single-ended only)

Table 8 – Bank 1 I/O Pins

Module Pin	FPGA Pin	XJTAG Net Name
135	T4	B2_0_N
137	P4	B2_0_P
141	R5	B2_2
		(single-ended only)
147	T6	B2_4_N
149	P6	B2_4_P
153	T7	B2_6_N
155	R7	B2_6_P
159	T8	B2_8_N
161	P8	B2_8_P
165	T9	B2_10_N
167	R9	B2_10_P
171	P12	B2_12_N
173	N12	B2_12_P

Module Pin	FPGA Pin	XJTAG Net Name
136	P5	B2_1_N
138	N5	B2_1_P
142	N6	B2_3_N
144	M6	B2_3_P
148	L7	B2_5_N
150	L8	B2_5_P
154	M7	B2_7_N
156	P7	B2_7_P
160	N8	B2_9
		(single-ended only)
166	P9	B2_11_N
168	N9	B2_11_P
172	M11	B2_13_N
174	M12	B2_13_P

Table 9 – Bank 2 I/O Pins

Module Pin	FPGA Pin	XJTAG Net Name
57	B3	B3_0 (single-ended only)
63	A2	B3_2_N
65	B2	B3_2_P
69	B1	B3_4_N
71	C1	B3_4_P
75	D1	B3_6_N
77	D3	B3_6_P
81	E1	B3_8_N
83	E2	B3_8_P
87	F1	B3_10_N
89	F2	B3_10_P
93	G1	B3_12_N
95	G3	B3_12_P
99	H1	B3_14_N
101	H2	B3_14_P
105	J1	B3_16_N
107	J3	B3_16_P
111	K1	B3_18_N
113	K2	B3_18_P
117	L1	B3_20_N
119	L3	B3_20_P
123	M1	B3_22_N
125	M2	B3_22_P
129	N1	B3_24_N
131	N3	B3_24_P

Module Pin	FPGA Pin	XJTAG Net Name
58	C2	B3_1_N
60	C3	B3_1_P
64	E3	B3_3_N
66	E4	B3_3_P
70	F3	B3_5_N
72	F4	B3_5_P
76	F5	B3_7_N
78	F6	B3_7_P
82	G5	B3_9_N
84	G6	B3_9_P
88	H3	B3_11_N
90	H4	B3_11_P
94	J4	B3_13_N
96	K3	B3_13_P
100	H5	B3_15_N
102	J6	B3_15_P
106	L5	B3_17_N
108	L4	B3_17_P
112	K6	B3_19_N
114	K5	B3_19_P
118	N4	B3_21_N
120	M5	B3_21_P
124	P1	B3_23_N
126	P2	B3_23_P
130	R1	B3_25_N
132	R2	B3_25_P

Table 10 – Bank 3 I/O Pins

6. I/O Voltage Domains

The supply voltage for each bank (V_{CC}) should be set according to the logic standard being used. Refer to Table 1 for the range of permissible voltages. The most common standards are listed in the following tables.

Some standards require the use of a reference voltage, which must be connected as indicated in Table 11. If any reference voltage input is not needed, the pin can be used as an additional I/O, although the capacitance on those pins (100 nF per connector pin) limits this to slow signals only.

Note that some I/O standards may require a 2.5 V Auxiliary supply. If you are using a logic standard other than LVCMOS, please refer to the Xilinx datasheets.

Module Pin	Signal	Comment	FPGA Pins for Alternative I/O[6]
30	VREF0	Reference voltage – Bank 0	A4, A12, C8
252	VREF1	Reference voltage – Bank 1	E12, L13
143	VREF2	Reference voltage – Bank 2	M10, T5
59	VREF3	Reference voltage – Bank 3	A3, M3

Table 11 – Reference Voltages Pinout

[6] For each bank, the alternative I/O pins listed are connected together on the module.

Standard	Min	Typ	Max	Units
LVCMOS33[7]	3	3.3	3.45	V
LVCMOS25[7]	2.3	2.5	2.7	V
LVCMOS18[7]	1.65	1.8	1.95	V
LVCMOS15[7]	1.4	1.5	1.6	V

Table 12 – Recommended V_{CC} for LVCMOS I/O

[7] These logic standards use an internal voltage reference and do not require an external VREF.

Standard	Min	Typ	Max	Units
LVDS_33[8]	3	3.3	3.45	V
LVDS_25[8]	2.25	2.5	2.75	V
BLVDS_25[8]	2.25	2.5	2.75	V

Table 13 – Recommended V_{CC} for LVDS Standards

[8] These logic standards use an internal voltage reference and do not require an external VREF.

7. I/O Current Capabilities

The maximum current capability of the pins is dependent on the drive strength set when the FPGA is configured. Possible options are listed in Table 14; they are dependent on the I/O interface voltage being used.

Voltage Domain	Output Drive Strengths (mA)	
	Banks 0, 1, 3	Bank 2
3V3	2, 4, 6, 8, 12, 16, 24	2, 4, 6, 8, 12, 16, 24
2V5	2, 4, 6, 8, 12, 16, 24	2, 4, 6, 8, 12, 16
1V8	2, 4, 6, 8, 12, 16, 24	2, 4, 6, 8, 12, 16
1V5	2, 4, 6, 8, 12, 16	N/A[9]

Table 14 – Maximum Output Current for LVCMOS I/O

[9] Bank 2 cannot be used with a 1V5 supply.

8. Configuring the FPGA

The module is fitted with a Xilinx® Spartan®-6 SLX16 FPGA in a 256-pin footprint. It can be configured over the JTAG interface or from the module's flash memory.

The board's LED indicates that the FPGA has been configured. When the image comes from the on-board flash memory, the LED should illuminate shortly after power-up; if the board is unprogrammed, the LED will remain off.

If you have a test setup where the FPGA needs to be configured, it is advisable for the associated XJEase tests to check the FPGA and to automatically commence programming if it's found to be unconfigured. XJTAG can supply the module together with an XJDeveloper board file and the associated XJEase files to provide this functionality. (NB: when used as a mini I/O board, no programming is needed.)

9. Mechanical

The module interfaces to a 260 pin SODIMM connector and requires a stack height of at least 4.0 mm.

Board dimensions:
69.6 ± 0.10 mm x 30.0 ± 0.15 mm

Figure 4 – Module Pinout