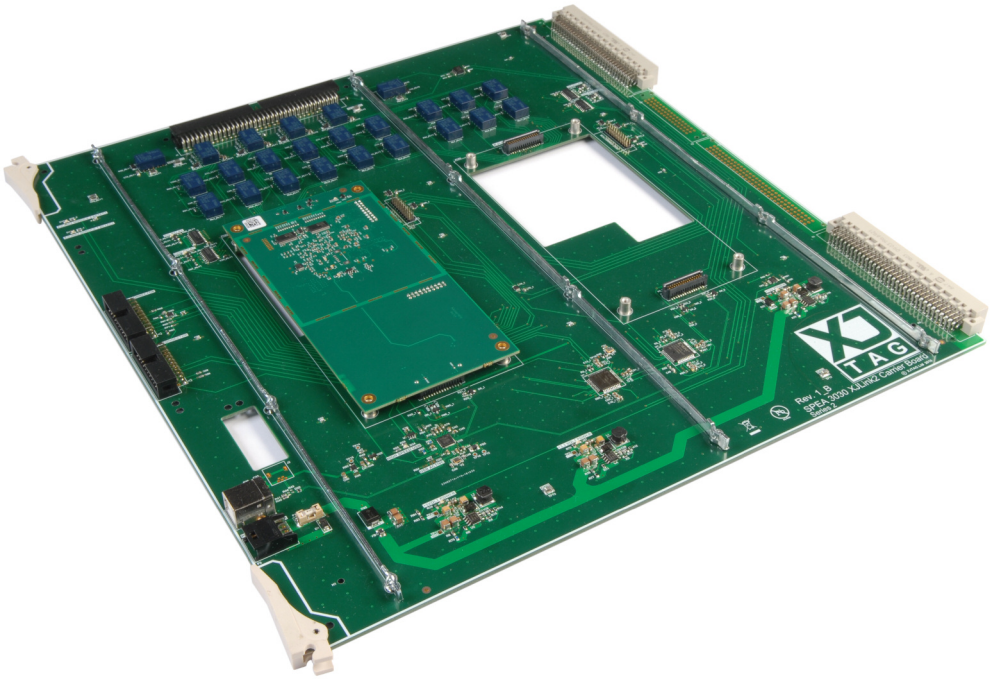
SPEA 3030
XJLink2 Carrier Board

User Guide

Version 1



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1. Introduction

The SPEA 3030 XJLink2 Carrier Board, hereafter called the Carrier Board, is XJTAG's recommended hardware solution for adding XJTAG boundary scan test capability to a SPEA 3030 bed of nails test system.

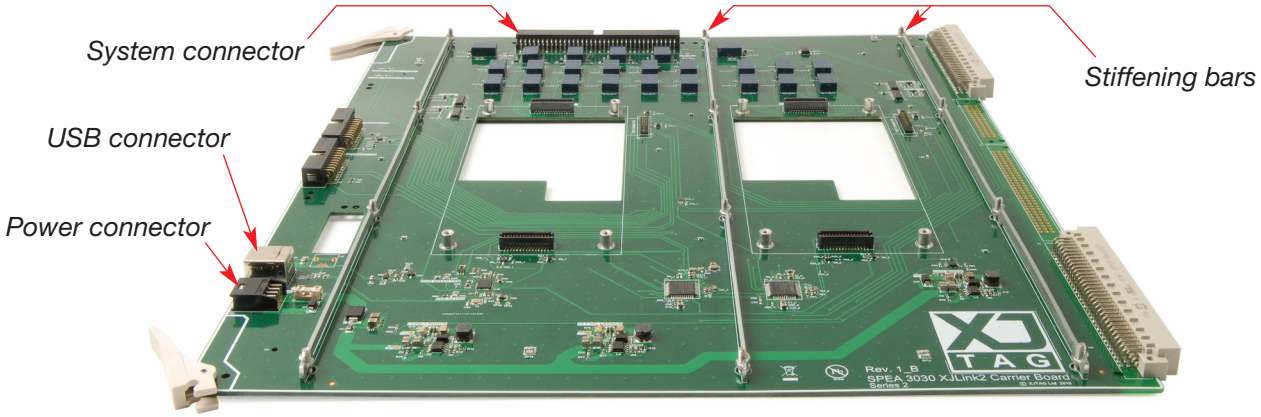


Figure 1 – Carrier Board with no XJLink2-3030 modules fitted

The Carrier Board is used in conjunction with XJLink2-3030 JTAG controller modules. It can support up to two independent modules and can operate with either one or two modules fitted. Each module is used to test a separate Unit Under Test (UUT) – modules cannot be used together for additional access on a single UUT.

2. System Overview

Figure 2 shows a simple block diagram of the Carrier Board and all the required connections. The external PSU provides all of the power that is needed for both the Carrier Board itself and any connected XJLink2-3030 modules. The USB connection is linked via an on-board hub to the XJLink2-3030 module sockets.

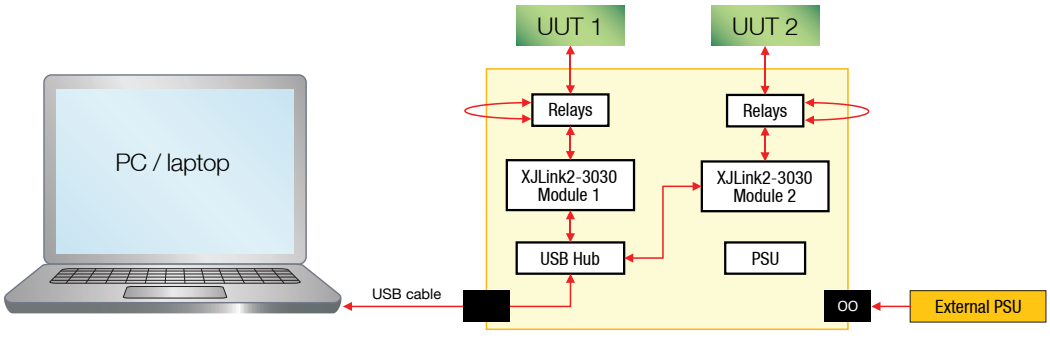


Figure 2 – Carrier Board block diagram

The UUT connections go from the XJLink2-3030 module to the UUT via relays on the Carrier Board. This ensures that the UUT is completely isolated from the XJTAG system during stand-alone bed-of-nails testing in the SPEA 3030 ICT test phase.

During XJTAG testing, including boundary scan/ICT integrated testing the relays are controlled to connect the pins (both signal pins and ground connections) of the XJLink2-3030 module to the UUT.

3. XJLink2-3030 Module Installation

Please follow normal anti-static handling procedures at all times.

Make sure that the board stiffening bars have been fitted (see *Figure 1* earlier), and that the Carrier Board is fully supported when each XJLink2-3030 module is inserted. Failure to do so could result in damage to the Carrier Board.

Remove the screws and washers used for securing the XJLink2-3030 module(s) from the Carrier Board, retaining them to secure the module after it has been inserted. Carefully align the connectors on the XJLink2-3030 module with the connectors on the Carrier Board (see *Figure 4* for the correct orientation of the module) before firmly pressing downwards until the module touches the four mounting screw points on the Carrier Board. Reinsert the screws taking care to keep the washers in the correct order (XJLink-3030/fibre washer/metal washer/screw), as shown in *Figure 3* below.

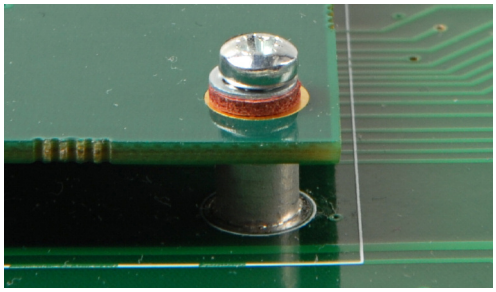


Figure 3 – Screw and washer assembly for fitting an XJLink2-3030 module

Figure 4 below shows a Carrier Board with an XJLink2-3030 module installed. If only a single XJLink2-3030 module is going to be used it is recommended that it be fitted as module 1. However as each module connects to pre-defined pins on the system connector, the XJLink2-3030 module must be installed in the correct slot for the fixture being used.

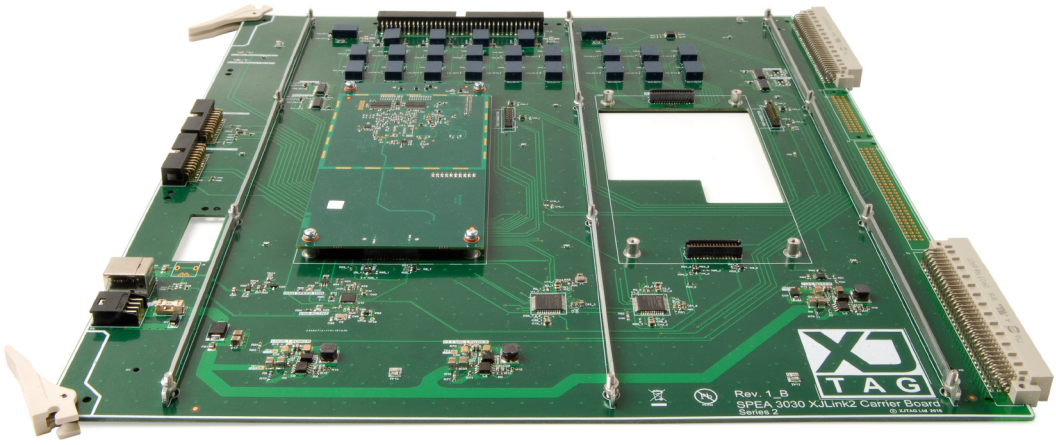


Figure 4 – Carrier Board with a single XJLink2-3030 module installed

4. Carrier Board Installation

The Carrier Board is installed into the backplane of the SPEA 3030 bed-of-nails tester. It requires separate connections for power and USB. Both of the required cables are supplied with the Carrier Board.

The Carrier Board is designed to be powered by a 24 Volt supply.
Please refer to the SPEA use and maintenance manual for detailed instructions on the physical installation.

5. Connecting a UUT to the Carrier Board

UUTs are connected to the Carrier Board using the 72-pin system connector (J1). As shown in *Table 1* below, this connector is split equally between the two XJLink2-3030 modules with pins 1-36 used for the connections to the module 1 and pins 37-72 used for the connections to the module 2.

	XJTAG pin mapping configuration pin	SPEA system connector (J1)		
		XJLink2-3030 (module 1)	XJLink2-3030 (module 2)	
GND	Pin 10	2, 3, 6, 7, 10, 11, 14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34, 35	38, 39, 42, 43, 46, 47, 50, 51, 54, 55, 58, 59, 62, 63, 66, 67, 70, 71	
GND	Pin 20			
Signal 1	Pin 1	1 (IO1_1 - RFU)	37 (IO2_1 - RFU)	XJLink2-3030 Bank 1
Signal 2	Pin 2	4 (IO1_2)	40 (IO2_2)	
Signal 3	Pin 3	5 (IO1_3)	41 (IO2_3)	
Signal 4	Pin 4	8 (IO1_4)	44 (IO2_4)	
Signal 5	Pin 5	9 (IO1_5)	45 (IO2_5)	
Signal 6	Pin 6	12 (IO1_6)	48 (IO2_6)	
Signal 7	Pin 7	13 (IO1_7)	49 (IO2_7)	
Signal 8	Pin 8	16 (IO1_8)	52 (IO2_8)	
Signal 9	Pin 9	17 (IO1_9)	53 (IO2_9)	
Signal 10	Pin 11	20 (IO1_11)	56 (IO2_11)	XJLink2-3030 Bank 2
Signal 11	Pin 12	21 (IO1_12)	57 (IO2_12)	
Signal 12	Pin 13	24 (IO1_13)	60 (IO2_13)	
Signal 13	Pin 14	25 (IO1_14)	61 (IO2_14)	
Signal 14	Pin 15	28 (IO1_15)	64 (IO2_15)	
Signal 15	Pin 16	29 (IO1_16)	65 (IO2_16)	
Signal 16	Pin 17	32 (IO1_17)	68 (IO2_17)	
Signal 17	Pin 18	33 (IO1_18)	69 (IO2_18)	
Signal 18	Pin 19	36 (IO1_19)	72 (IO2_19)	

Table 1 – Main system connector J1 pinout (connects to UUT)

The two sets of system connector ground pins (one set for each module) are electrically isolated from one another. If both modules are being used, all of the ground pins will be connected together via the Carrier Board system ground when the tests are running.

When fabricating the connections from the UUT to the system connector, use twisted pair cables. Each active signal is located next to a ground signal on the system connector to make this easy to implement. To ensure optimum signal integrity all of the ground wires from the twisted pairs should be connected to ground test points as close to the active signals as possible on the UUT. If this is not done, large loop areas can occur – see Signal Integrity in Test Fixtures (PDF) for more details.

6. XJDeveloper Project Requirements

To use an XJLink2-3030 module in the Carrier Board to run boundary scan tests, the XJDeveloper project must control the relays at the start of the test sequence in order to make the connections between the UUT and the module.

The relay connections are activated when the function of pin 1 of the XJLink2-3030 is set to be "*Power On*". This is configured on the pin mapping screen in XJDeveloper.

This means that pin 1 cannot be used for any other function. It should also be noted that although IOx_01 signals are brought out to the system connector these pins are is currently reserved for future use; they will not be driven high and cannot be used to supply any power to the UUT.

Pin 11 must not be used for its *Power On* function. On the XJLink2-3030 module this function is again reserved for future use, it will not cause pin 11 to be driven high and the pin cannot be used to provide any power to the UUT.

Pin 11 can be used for any other function, as a TAP pin, a general purpose I/O pin or for frequency or voltage measurement.

7. Relay Connection Sequencing

When the XJTAG project is executed, either directly from XJRunner/XJDeveloper or from within SPEA Leonardo, the relays linking the system connector to the XJLink2-3030 modules are activated in a sequence.

The first relay to be connected gives a resistive ground connection to prevent any issues that could be caused by significant voltage differences between the Carrier Board system ground and the UUT ground.

The second relay connection is non-resistive ground to ensure a stable ground connection between the module and the UUT.

The third step in the sequence connects the IOx_xx signals between the XJLink2-3030 module and the system connector.

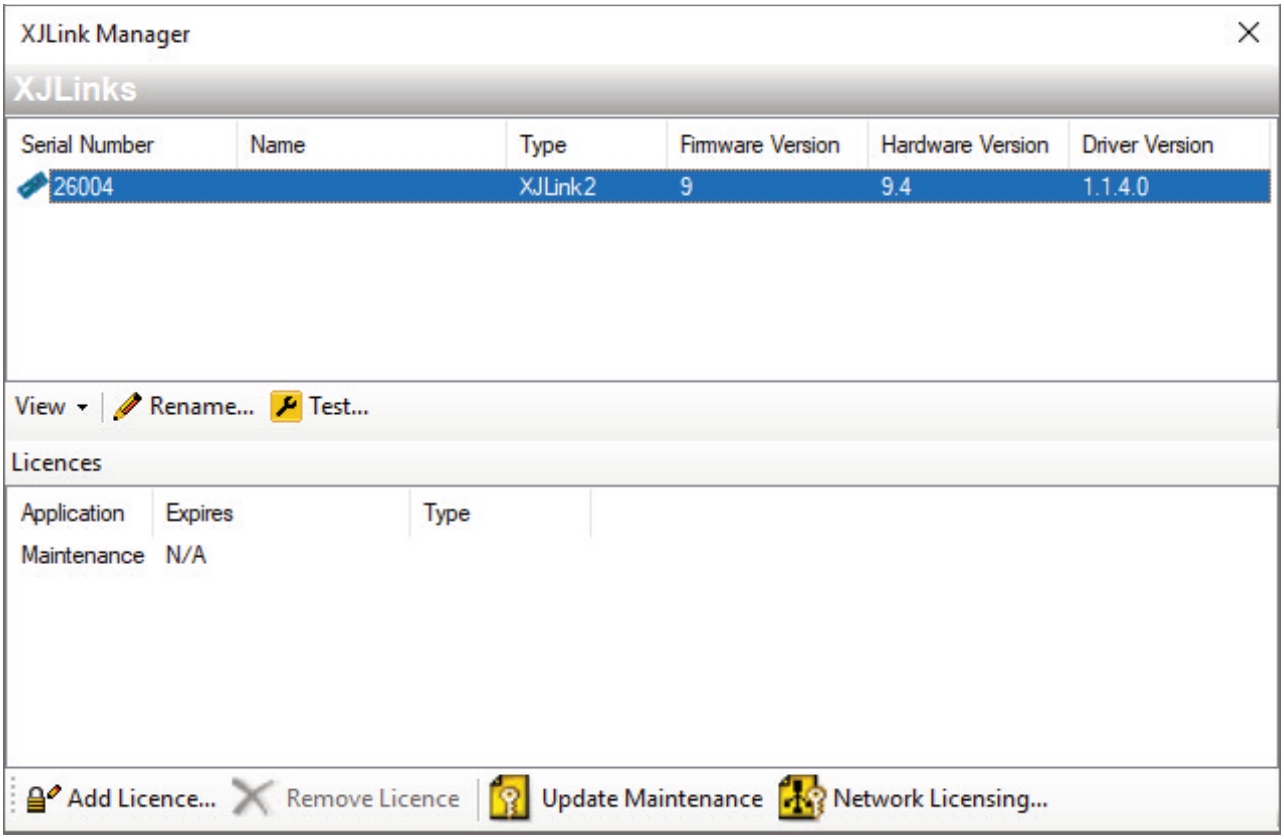
Once the JTAG testing is complete the relays return to their default state with the UUT fully isolated from the XJLink2-3030 module. The active signals are disconnected first and then both resistive and non-resistive ground connections are disconnected at the same time.

8. XJLink2-3030 Module Self-Test Configuration

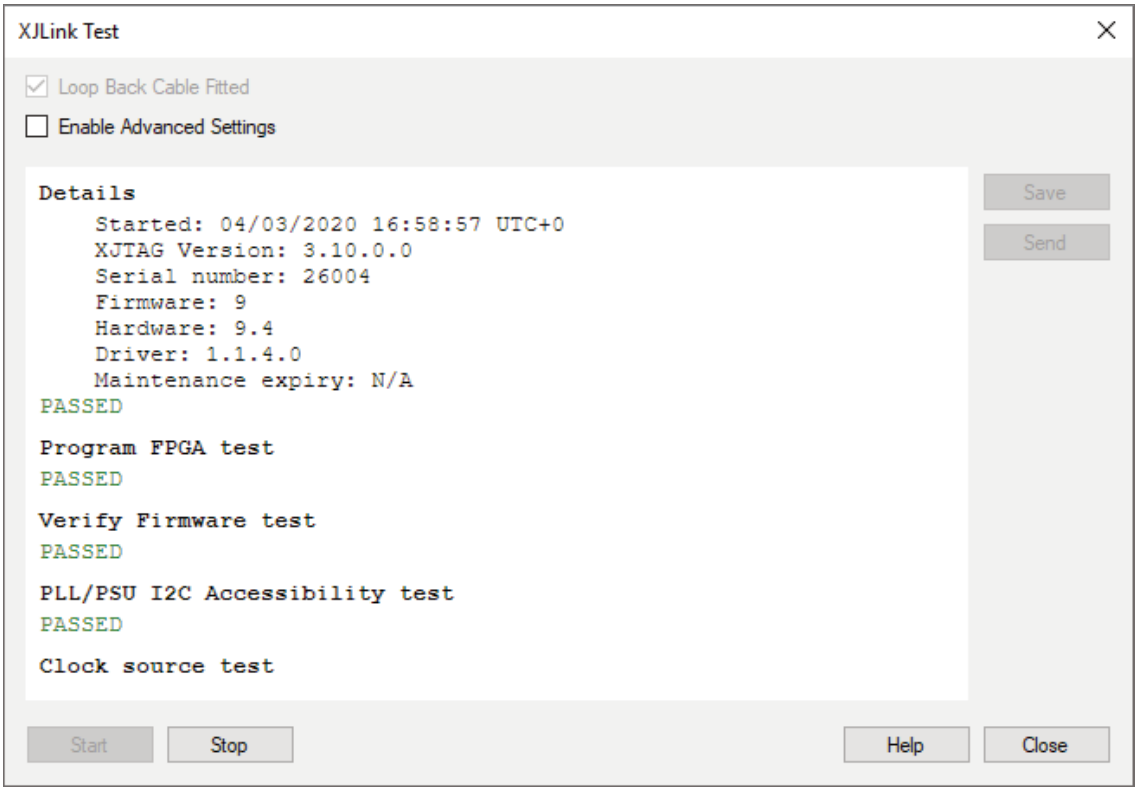
The relays used to isolate the UUT from the XJLink2-3030 modules also provide a built-in loopback between the module pins when the Carrier Board is in its default state, i.e. not actively running tests. This allows a self-test to be run on the XJLink2-3030 modules.

Running the self-test on an XJLink2-3030 module in the Carrier Board will automatically include loopback testing. The self-test can be launched from within the XJLink Manager or programmatically using the supplied XJIntegration DLL.

When running from the XJLink Manager, with the XJLink selected, simply click the "*Test…*" button to launch the XJLink test dialog.



The *Loop Back Cable Fitted* option is selected and greyed out as the Carrier Board will automatically apply the required loopback.



When running the self-test from the integration DLL use the Test method on the XJLink object specifying a value of true for the `runLoopBackTest` parameter.

9. Carrier Board Electrical and Operational Specifications

Outer dimensions (including connectors)	342 mm length x 369 mm width x 11 mm height
Nominal PSU operating Voltage	24 VDC (± 5%)
Minimum PSU operating Voltage	12 VDC
PSU source	External (SPEA 3030 system)
PSU Under voltage lockout value	Approximately 10 V
Current consumption (No modules in place)	Approximately 17 mA (24 VDC PSU input)
Current consumption (1 module, relays not active)	Approximately 41 mA (24 VDC PSU input)
Current consumption (2 modules, relays not active)	Approximately 64 mA (24 VDC PSU input)
XJLink2 data connection	Single approved USB cable (normal B-type)
Maximum number of fitted XJLink modules	2
System Test connector	72-way double-row right angle 0.1 inch pitch connector Digi-key # TSS-136-04-L-D-RA-ND

10. Handling Procedures

In all cases, it is assumed that the Carrier Boards and XJLink2-3030 modules are handled by personnel