PXI-XJLink2

Technical Specifications

Absolute Maximum Ratings

DC input voltage	–0.5 V to 5.5 V
DC input current	±10 mA
DC output current	(Pins 1, 11 with power on) +50 mA
	(NB capacitors > 10 µF connected to these pins should have current limiting circuitry fitted)
DC output current	–50 mA, +50 mA including power and ground pins
Temperature Range	+5 °C to +45 °C (operational)
Humidity	< 95% (non-condensing)

DC Electrical Characteristics

Output voltage programmable range: 1.1 V to 3.3 V in 0.1 V steps

Output voltage tolerance: ±5% of set value, typically ±3%

Bank Voltage	V_{IL} Max	V_{IH} Min	V_{OL} Max	V_{OH} Min	Load conditions
3.3	0.8	2.0	0.4	2.4	100 Ω
2.5	0.7	1.7	0.4	2.0	100 Ω
1.8	0.4	0.9	0.4	1.35	100 Ω
1.5	0.4	0.85	0.4	1.0	100 Ω
1.2	0.4	0.75	0.4	0.8	133 Ω

Variable Input threshold:

V_{IL} (Max) = V_{THRESH} – 0.14 V

V_{IH} (Min) = V_{THRESH} + 0.14 V

External V_{REF}:

$$V_{IL}\ (\text{Max}) = \frac{V_{REF}}{2} - 0.14\ \text{V}$$

$$V_{IH}\ (\text{Min}) = \frac{V_{REF}}{2} + 0.14\ \text{V}$$

TCK Frequency

10 kHz to 166 MHz in steps of 0.05 MHz.
Autoskew compensates for the delay introduced by the cable and the JTAG devices by up to 3 TCK periods.

Visual Indication

Red light:	Test FAILED
Yellow flashing light:	Test RUNNING
Green light:	Test PASSED

Frequency Counter

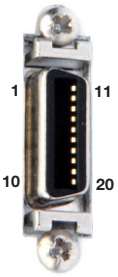
	Min	Max
Frequency Input	1 Hz	200 MHz
Accuracy	±10 ppm	

Selectable measurement period: 1 ms, 10 ms, 100 ms, 1 s, 10 s

Voltage Measurement

	Min	Max
Voltage Input	0	5 V
Accuracy	±(0.2% + 10 mV) @ 15 °C to 35 °C	
Input impedance	> 900 Ω	

JTAG Connector



3M 20-way MDR Receptacle.
Manufacturer's part number: 10220-5212PL.

The cable supplied with the XJLink2-PXI is made from the following Farnell components:
Part No. 929-2675, 929-2969, 109-9239, 117-0221.

Example supplier part codes for mating IDC plug:
Digikey MPB20A-ND, RS 163-3285, Farnell 9292675.

Configurable JTAG Connector Pinout

I/O1	1	11	I/O11
I/O2	2	12	I/O12
I/O3	3	13	I/O13
I/O4	4	14	I/O14
I/O5	5	15	I/O15
I/O6	6	16	I/O16
I/O7	7	17	I/O17
I/O8	8	18	I/O18
I/O9	9	19	I/O19
GND	10	20	GND

Each of the 18 interface pins can be configured to be any one of the JTAG signals that make up the IEEE 1149.1 TAP controller interface.

Dimensions: 1 PXI slot