XJAccelerator v1

Overview

This is the previous version of the XJAccelerator, now only available for legacy project support. XJAccelerator v1 is a multipurpose unit that can be integrated with your XJTAG system to facilitate and accelerate programming functions as well as extending test coverage on a Device Under Test (DUT).

JTAG controlled programmer

Based on a Xilinx Spartan 6 FPGA, the XJAccelerator v1 card is principally designed to provide a versatile platform for accelerated programming applications. In this mode the FPGA is configured with XJFlash to program flash devices connected to any of the three I/O headers. The data to be programmed can either be streamed into the unit over JTAG or retrieved from a microSD card using the slot provided.

The FPGA can either be configured through its JTAG port, as part of a standard XJTAG project, or from the on-board PROM. To minimise the total time required for each board, the configuration status of the FPGA is checked each time the project is run. Only if an unexpected status is found will the FPGA, or the configuration PROM be programmed.

Versatile and reconfigurable

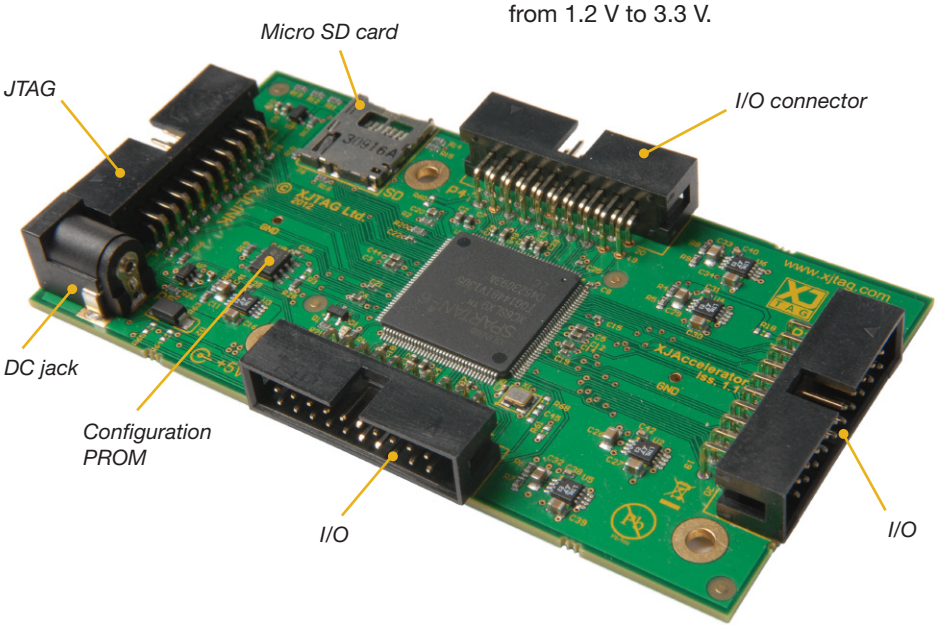
The XJAccelerator v1 card can be used to program standard NOR and NAND flash devices provided it is given access to all of the required signals. More bespoke programming operations are also possible providing the programing protocol can be replicated by the FPGA.

XJTAG can provide XJFlash images that implement the following protocols:

- **SPI** – Serial Peripheral Interface
- **I²C/IIC** – Philips/NXP Semiconductor's Inter-IC bus
- **ICSP** – Microchip's In-Circuit Serial Programming
- **SWD** – ARM's Serial Wire Debug

If the protocol you require is not listed here please contact us and we will be happy to investigate the possibility of adding that capability.

The unit is powered by an external 5V supply. The voltage levels for the three I/O connectors are user configurable from 1.2 V to 3.3 V.



Key Benefit

- Fast flash programming
- Increases board test coverage with additional interface connectivity
- Easy integration with XJTAG test systems

Features

- Reconfigurable
- FPGA board
- Supports SPI, IIC, ICSP, SWD and other protocols
- Supports NOR and NAND flash devices

Digital I/O testing

It is also possible to use the boundary scan capabilities of any unused signals on the three I/O headers for external digital I/O testing on a DUT.

Flexible connection

The XJAccelerator v1 card can be connected to the JTAG controller in a number of different configurations allowing easy integration into a wide range of projects. It can be connected to a separate TAP on an XJLink2-based JTAG controller or added in series with the JTAG chain of the DUT.

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