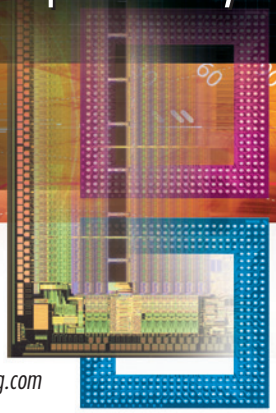
Using the JTAG Chain for Accurate System and Intra-Die Power and Thermal Analysis

New boundary scan techniques using Xilinx System Monitor test more aspects of system behavior.



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Engineers typically use the boundary scan chain to program devices such as CPLDs or flash memories. But more engineers should be tapping into the power of boundary scan as a way of extracting detailed information about how boards or systems are functioning.

With the recent introduction of the Xilinx® System Monitor function inside the latest Virtex™-5 FPGAs, you can now collect voltage and temperature information from within the FPGA using the same Joint Test Action Group (JTAG) test access port (TAP) traditionally used for boundary scan functions and programming devices.

And by using equipment and test scripts provided by Xilinx partner XJTAG, or by writing your own scripts, you can more easily verify analog signals at various points in the circuit from within the boundary scan test environment. XJTAG's boundary scan test system helps engineers test devices such as discrete temperature sensors, DACs, or VGA ports.

System Monitor: A Device-Level Test Probe

The System Monitor is analog circuitry within the Xilinx Virtex-5 FPGA architecture that samples on-chip temperature and voltage (Figure 1). The dedicated System Monitor circuitry – which is built around a 200-ksps ADC by default – performs a continuous sequence of measurements on the FPGA die temperature, as well as V_{CCINT} and V_{CCAUX} supply voltage levels. This feature in Virtex-5 devices eliminates the added complexity and cost of implementing external monitoring components to a system.

Moreover, the System Monitor feature allows you to take power supply measurements from the die itself (inside the package), which is not possible using an external ADC.

You can also use System Monitor to get accurate thermal readings. Traditionally, engineers used thermal diodes to monitor die temperatures, but they had to pay careful attention to the PCB layout because diode measurements are highly sensitive to noise from other devices and features on the PCB, as well as other implementation details such as signal offsets and tolerances. The new System Monitor gets around that issue. It incorporates a temperature sensor on the FPGA die to allow you to take accurate temperature readings from the die itself (Figure 2).

These power and thermal monitoring capabilities allow for the implementation of safety functions such as power-on self-check or over-temperature power down. System Monitor's internal power supply measurements are accurate to within ±1%, while monitoring of the on-chip temperature sensor is accurate to ±4 °C in the -40 °C to 125 °C range.

The System Monitor circuitry also includes an integrated multiplexer that not only supports inputs for the two on-chip voltage-sensing channels and temperature sensor, but also accepts inputs from as many as 17 additional analog sources external to the FPGA. This means that you can use System Monitor to monitor various off-chip analog signals. It supports off-chip inputs that are single-ended or differential signals, up to 1.0V in amplitude; thus, you can connect to many types of sensors, including shunt resistor-based current sen-

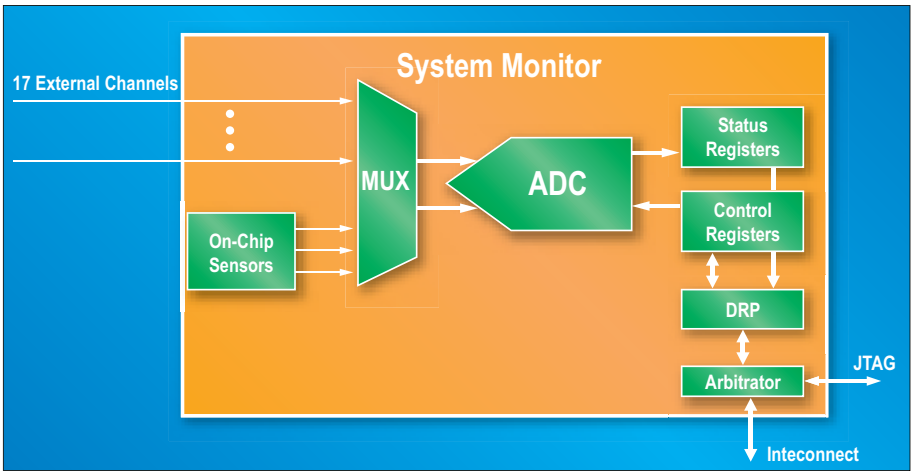

Figure 1 – System Monitor allows you to monitor voltages and temperature of a Virtex-5 FPGA die and as many as 17 other analog sources that can impact overall system performance.

sors, accelerometers, position sensors, and external temperature sensors.

The System Monitor control system also includes an automatic channel sequencer that allows you to define which parameters you want to monitor. You configure System Monitor by setting up its control registers. To do this, simply instantiate System Monitor in your design or write to the control registers over JTAG. The Xilinx ISE™ software tool suite also includes a utility called the System Monitor architecture wizard to walk you through the instantiation process.

Turning on the TAP

By designing System Monitor to deliver this data directly to the FPGA's JTAG TAP, Xilinx has opened up many new opportunities for extracting detailed information from prototype or production systems. Moreover, you can import the data into boundary scan test gear that operates at a high level of abstraction.

Although most engineers are familiar with using boundary scan to program devices in situ, many remain unaware of its power as an unobtrusive debugging and test solution. Applying tests through the JTAG TAP means that you no longer need to physically attach test probes to a development board or production assembly. Attaching probes is time-consuming and leaves the test strategy vulnerable to errors.

More importantly, it is impossible to physically probe modern BGA- and CSP-type device packages because the ball pitch is so fine and is located under the device's body. And as the industry increasingly uses these packages in new ICs, it is effectively reducing the amount of test coverage you can achieve using conventional test techniques.

Boundary scan testing, as defined by the Joint Test Action Group and ratified as IEEE1149.1, specifies a four-wire TAP and boundary scan architecture that engineers can implement in their IC designs to facilitate product testing later in the IC development cycle. The four-wire TAP interface allows engineers to read values into and out of pins or internal registers of JTAG devices. And with access to these pins, you can debug and test other devices on the circuit board, such as FPGAs, EEPROMs, RAMs, and flash memory.

Using boundary scan test equipment, you can perform quick net-level diagnostics without having to rely on embedded test software or functional tests. The PCB doesn't need to be running for you to use it, so you can quickly verify basic functionality as soon as first prototypes return from assembly, even if the board will not boot up. You can also carry out basic checks, toggling individual pins or buses

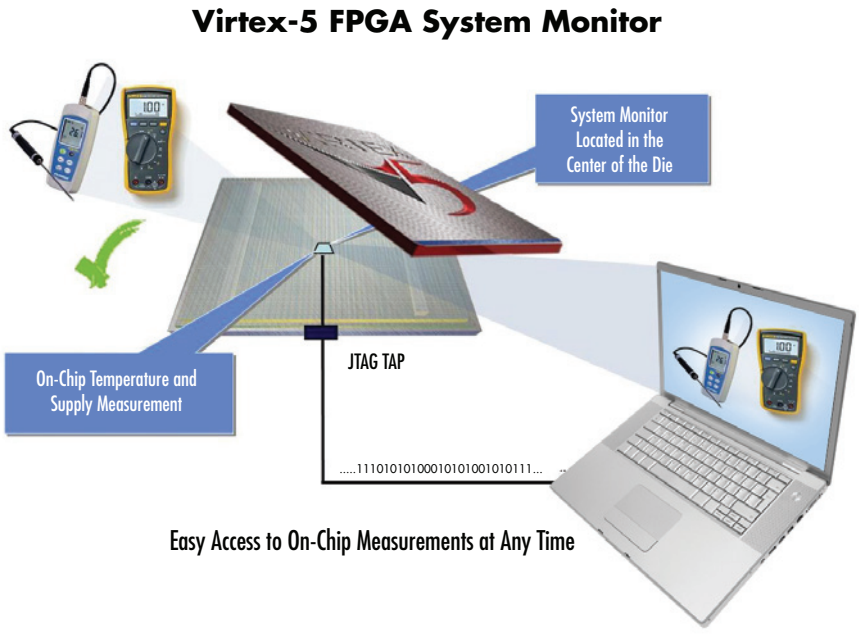

Figure 2 – The System Monitor sensor, located in the center of the Virtex-5 device die, provides valuable on-chip voltage and temperature data accessible during product development, when the device is in mass production, or even after deployment in the field.

Engineers at XJTAG, working with Xilinx and the Virtex-5 LXT ML505 development board, developed several turnkey test scripts that allow XJTAG boundary scan test solution users to access data from System Monitor.

to locate shorts, breaks, poor joints, or incorrect connections.

The test ports of all JTAG devices in the system are interconnected at the board level, setting up a serial scan chain that you can access through a single connector at the edge of the board. As the numbers of JTAG-compliant devices per board increase, emerging JTAG testers can access a greater proportion of the total nets, thereby increasing overall test coverage.

By manipulating the scan chain to set up suitable test patterns, you can also collect responses from components that do not offer a boundary scan test interface, provided that the components you want to access are connected to the same net as a compliant device. This technique is sometimes referred to as cluster testing, and provides a way to test non-JTAG devices such as external connectors, video chips, IIC devices, Ethernet controllers, LEDs, or switches.

For example, you can also use the JTAG chain to drive an Ethernet test packet to a non-JTAG Ethernet controller on the board and verify its response (Figure 3). Similarly, it is possible to test SRAM devices, as well as SDRAM, DDR, and DDR2 chips – even though these are not JTAG-enabled. These examples show how modern boundary scan equipment, such as the XJTAG system, has raised achievable test coverage by using the JTAG chain to its maximum potential. In practice, XJTAG customers are now achieving more than 90% test coverage for complex boards.

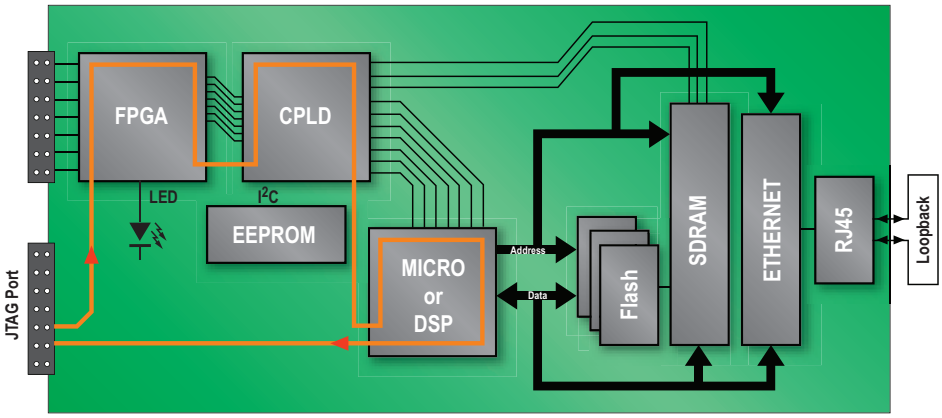

Figure 3 – Thanks to the growing JTAG compliance in modern PCB design, you can use boundary scan to perform many more types of tasks and tests.

Extending Boundary Scan Capabilities

Now that Xilinx System Monitor allows you to easily collect analog values from inside Virtex-5 FPGAs, those of you already familiar with boundary scan testing can apply yet another valuable set of tests through the TAP. Virtex-5 device users can import data from the 17 external analog channels into the boundary scan test environment through System Monitor.

The use of the Virtex-5 System Monitor feature requires PCB design engineers to follow a certain minimal set of design guidelines. These guidelines are documented in the applications section of the Virtex-5 System Monitor User Guide (*www.xilinx.com/support/documentation/user_guides/ug192.pdf*).

Once the PCB support is in place, it's time to take advantage of System Monitor's many capabilities. For example, because the System Monitor ADC is operational on power-up, you can extract valuable system information using the boundary scan chain even before configuring the FPGA. This allows development engineers, for example, to verify system power rails and assess basic cooling provisions before finalizing the FPGA configuration.

Because Xilinx implemented the sampling circuitry in hardware on the FPGA silicon, you can apply the System Monitor functions at any time in the product lifecycle. For example, if a system exhibits persistent overheating or if a power supply starts to exhibit signs that it is defective in the lab or even in the field, you can immediately apply a test to read the System Monitor data through the JTAG TAP without reconfiguring the FPGA.

XJTAG Simplifies Emerging Uses of Boundary Scan

Engineers at XJTAG, working with Xilinx and the Virtex-5 LXT ML505 development board, developed several turnkey test scripts that allow XJTAG boundary scan test solution users to access data from System Monitor. XJTAG can display die temperature, supply voltages, and off-chip analog values directly onto a workstation, and it allows you to verify that the values System Monitor and XJTAG collect are within specified tolerances.

Figure 4 is a code snippet of a simple set of tests that users can generate in XJTAG's high-level scripting language, XJEase, to check the operating parameters of the Virtex-5 FPGA. In the function call `Test`, you first configure System Monitor. The test then reads individual inputs and checks them.

Figure 5 shows code that checks the device's temperature. If the temperature is out of tolerances, the test displays an error. This example shows how you can access Virtex-5 System Monitor using simple functions provided on the XJTAG website.

XJTAG also supports customized tests that can, for example, record System

Monitor data for fault detection or traceability purposes. You can also write scripts to have XJTAG check for peak values, respond to thresholds, or apply an averaging algorithm to the data from System Monitor.

```
//----------------------------
Test()(INT result)
//----------------------------
INT temp;
  result := 0;

  Config_SysMon()();

  Read_Internal_Temp()(result);
  Read_VAUX()(result);
  Read_VINT()(result);
  Read_RefP()(result);
  Read_RefN()(result);

  IF (result != 0) THEN
    result := RESULT_FAIL;
  ELSE
    result := RESULT_PASS;
  END;

END;
```

Figure 4 – Code snippet showing how to set up and test some of the System Monitor inputs using the XJEase scripting language.

You can create scripts using XJEase, which XJTAG includes as part of the XJTAG environment. XJEase allows you to work at a high level of abstraction from the raw boundary scan data. You can also write test scripts specifically for devices, whether or not the devices are in the boundary scan chain. You can store these scripts and even reuse them for future projects.

XJTAG will generate a new test sequence automatically each time the netlist data indicates a change to the board, which saves you from manually rewriting the test routine. In contrast, older types of boundary scan test equipment typically produce board-centric test sequences that are laborious to update with each design change.

As this device-centric scan approach to test development increases in popularity within the engineering community, many XJTAG users have begun posting their proven pre-written scripts on XJTAG's website. Customers who have current support contracts with XJTAG can download these scripts from *www.xjtag.com* free of charge and incorporate them into their test routines. And if the website does not have the exact device you are looking for, simply download a similar script and customize it for the device you want to test.

Scanning the Future

The scope of the interactions possible between System Monitor and XJTAG highlights the potential for boundary scan test systems to support innovative on-chip features supporting verification, debugging, parameterization, and calibration. By accessing silicon features implemented in the core of FPGAs – or other devices such as processors, memories, or control ICs – it becomes possible for boundary scan to perform functions such as virtualizing DIP switches, calibrating digital filters, or adjusting analog settings or threshold values. Plus, you can now achieve this quickly, whether the product is at the development stage, in volume production, or operating in the field.

For engineers already using the boundary scan chain to test the functional nets of prototype or production assemblies, System Monitor now allows vital-signs monitoring from within the boundary scan environment. Those of you who are more ambitious will certainly step up and take advantage of this new ability to see even more deeply into the system. And in the future, as the technique becomes more mainstream, expect to see customized test scripts that reach into even the most inaccessible aspects of product designs.

```
//-------------------------------------------------------------------------------
Read_Internal_Temp()(INT result)
//-------------------------------------------------------------------------------
  INT temp;
  Read_Temp()(temp);
   IF ((temp < (Die_Temp - Temp_Margin)) || (temp > (Die_Temp + Temp_Margin))) THEN
    PRINT("Die temperature = ",temp,"C.  ** OUTSIDE LIMITS **\n");
    result := result + 1;
  ELSIF (DEBUG) THEN
    PRINT("Die temperature = ",temp,"C\n");
  END;
END;

//-------------------------------------------------------------------------------
Read_Temp()(INT temp)
//-------------------------------------------------------------------------------
  Read_Channel(0)(temp);
  temp := ((temp * 20159) / 40960) - 273;
END;
```

Figure 5 – Code snippet for testing the temperature of the Virtex-5 FPGA