



# JTAG Integrated with PCB Design Tools Broadens Capabilities

By Philip Ling

Many engineers think that JTAG is simply an interface for inserting breakpoints to debug the software running on a CPU. It may surprise them to learn that JTAG is included in many integrated devices that do not have a debug interface. While this includes FPGAs and CPUs, it also extends to memory, communication interfaces and even general logic devices.

JTAG is so prevalent that in the majority of designs there will be at least one JTAG device on a board, and even a single JTAG-compliant device can be enough to make significant test coverage possible.

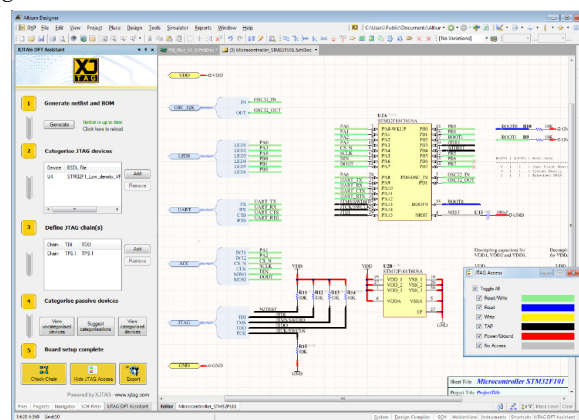
Boundary scan is not limited to testing JTAG-enabled devices, however. This is one of its greatest strengths and is a fundamental feature. With appropriate software, it enables the testing of nets between JTAG and non-JTAG devices on a PCB, or even across multiple PCBs in a larger system.

In this way it is able to detect a range of conditions, such as open circuits, missing components and short circuits between nets. It can also determine stuck-at faults (nets that remain

high or low) and provide probable fault locations.

## Testing with JTAG

Committing to JTAG boundary scan at the schematic capture stage not only provides validation before a PCB is produced, but provides tests that can be run as soon as the prototype arrives, without the need for rushed functional tests.



**Boundary scan software extension showing test coverage in Altium Designer.**

It is important in design to make sure the JTAG scan chain is connected and terminated correctly. As most PCBs

are now designed using CAD tools, it is encouraging to know that tool vendors are now integrating support for verifying JTAG scan chains at the PCB design stage. A good example of this is Altium Designer, a design environment that now supports plug-ins from XJTAG and JTAG Technologies.

These plug-ins support the verification of JTAG scan chains and show the level of test coverage that can be achieved using JTAG on a given PCB. XJTAG has also recently released a version of its plug-in (XJTAG DFT Assistant) for the OrCAD Capture PCB design environment. These developments show that JTAG is becoming more important to OEMs to meet both engineering and commercial objectives. In turn, design engineers are supported in making their designs more testable.

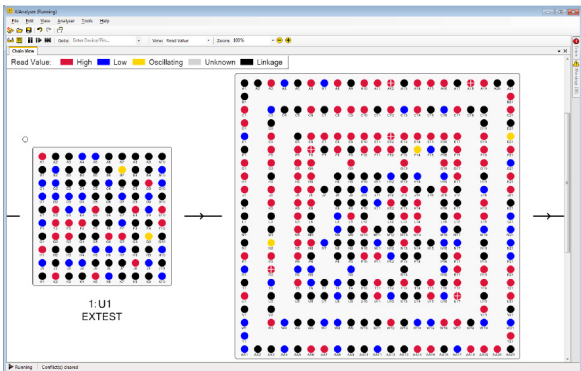
## Overcoming Test Challenges

Investment in design for test (DfT) early in the design stage often pays dividends, saving time and cost throughout the product development cycle. Typically, design rules are applied at the PCB design stage and are closely linked to design for manufacture (DfM)

rules, such as the proximities of components.

Ideally, test access points would be provided for every net on a PCB. This has never been possible, but what should be apparent from the trend towards greater integration and smaller packages is that providing test access points is becoming increasingly difficult.

Nets that start and terminate beneath a BGA remain completely inaccessible to physical probing unless a dedicated test point is added, which can



***JTAG test access is achieved electronically through pins, not test points.***

significantly increase the routing burden and add to signal integrity and EMC issues.

It is not surprising that, as a result, test access is declining. Test coverage, however, is growing in importance, as devices get more complex. Many manufacturers now agree that using JTAG for connectivity testing is becoming important in the quest for better test access, because it is unaffected by rising pin densities.

Using JTAG, test access is achieved electronically through pins, not test points. It is not limited by physical access, all it needs is one point of access to the board and a properly connected and terminated JTAG scan chain.

### JTAG's Relevancy

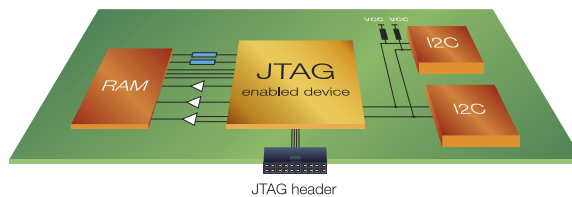
Created by the Joint Test Action Group, the term JTAG is often used interchangeably with the standard's

official title IEEE Std 1149.1. Most engineers will be familiar with the JTAG interface as it is the way the majority of in-circuit debugging probes connect to microcontrollers. Some will understand how this relates to boundary scan testing but not all will make use of its features.

As package sizes shrink, packing the same or greater functionality into a smaller area results in an increase in pin count and density. An example of this is the wafer-level chip scale package (WL-CSP) which can have a ball pitch of just 0.4 mm (0.016 in.), yielding around 25 balls in just 2 mm<sup>2</sup> (0.003 in.<sup>2</sup>). Although this enables end products to be significantly smaller, it does present design, test and manufacture challenges at the PCB level.

This is an ongoing challenge; it emerged with the introduction of multilayer boards, surface mount devices and the ball grid array (BGA) package. The physical contacts of a BGA device are largely inaccessible to test probes. The way the semiconductor industry addressed this challenge was through JTAG.

JTAG is foremost a technology designed for test purposes, as opposed to debug. It was originally conceived, developed and adopted by semiconduc-



***JTAG is also used to test non-JTAG devices.***

tor vendors in order to provide a method for reading and driving the logic level on each pin of a device. The features related to testing are the mandatory features of JTAG boundary scan — the ones that device manufacturers must implement in order to be compliant with the IEEE

1149.1 standard.

JTAG effectively turns the pins on a JTAG-enabled component into test access points, providing a gateway to allow JTAG testing of the connected nets, including non-JTAG devices, even if only one component on the board is JTAG-enabled.

### A Standard for the Future

Although it is predominantly intended to test nets on a PCB, JTAG is also used to carry out testing of non-JTAG devices on a board. Through manipulating the logic levels of digital devices, tests can be performed on any accessible device on a PCB. These test capabilities are provided by boundary scan specialist companies, along with many additional features including the ability to program devices in-system.

The JTAG standard is also evolving to address new challenges, with updates to IEEE Std.1149.1 and related standards, including IEEE Std.1149.6 (testing AC coupled and/or differential signals) and IEEE Std.1149.7 (which introduced enhanced features and support for reduced pin count), and active working groups discussing further additions to the capability of boundary scan.

Boundary scan is a rare thing — an established technology that still has much more to offer. In fact, it is becoming more significant with time, without needing to change in any disruptive way. It is already present in the majority of PCB designs.

Recent collaborations between the boundary scan and EDA vendors mean that getting access to the benefits of JTAG is as simple as downloading a free plug-in or extension to the schematic capture tool. JTAG's longevity isn't an accident; it was conceived with tomorrow's challenges in mind.

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