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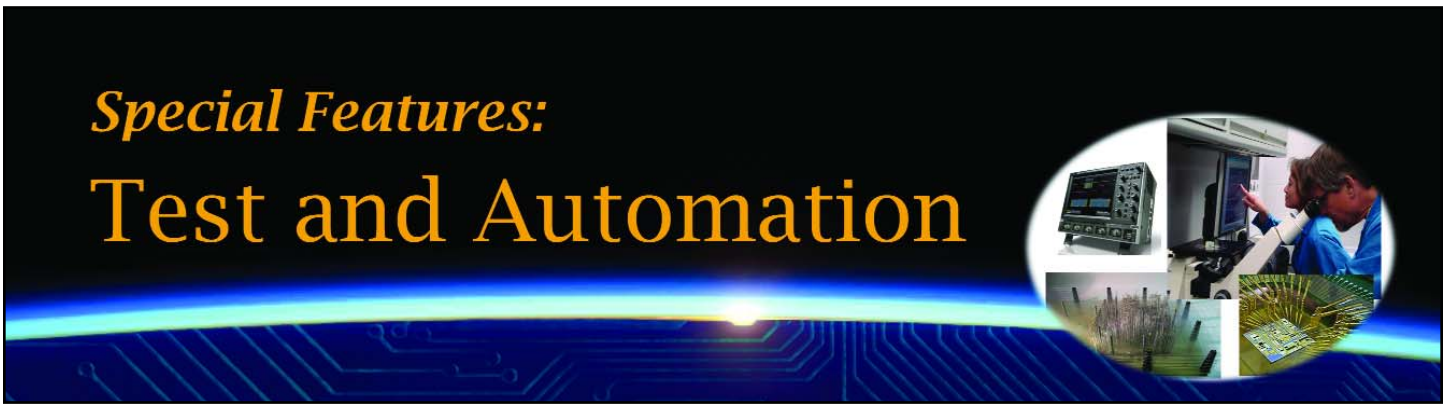

Beyond Debug: XJTAG for Flash Programming and Board Test

By Philip Ling

The JTAG standard, first established by the IEEE 27 years ago, defines an electrical and physical method for connecting JTAG-enabled devices on a PCB, or across multiple PCBs. However, JTAG is not a general-purpose bus. The technology behind the interface differs significantly from a standard communications interface.

The JTAG subsystem inside a JTAG-enabled device is empowered to take control of the pins of that device. In this mode the device's primary functions are suspended, enabling the JTAG subsystem to assert or read each pin's logic level, in response to messages sent over the JTAG scan chain.

It effectively turns every pin on the device into a virtual test point, accessed electronically, which is extremely useful for debugging a prototype board. These virtual test points, accessible without a dedicated test fixture, mean that even first prototypes can be tested using JTAG, on a bench or even by the manufacturer.

Each device in the scan chain is characterized by a description file written in boundary scan descriptive language (BSDL). Silicon vendors provide a free BSDL file for each type of JTAG-enabled chip. This file describes the JTAG capabilities of the device.

Test data sent to the JTAG scan chain is serially clocked in and out of each device, typically at several MHz. The speed at which boundary scan tests can operate often comes down to how well the

JTAG goes beyond being simply a debug interface, and can perform flash programming as well as a range of tests.

scan chain has been implemented on the PCB in terms of signal integrity, as well as the capability and efficiency of the test equipment used. This is how JTAG tool providers are able to differentiate themselves, in how well their technology can generate test patterns, apply those tests, interpret the results and reformulate new test patterns to identify and isolate fault conditions quickly.

JTAG for Test

Automated test equipment (ATE), such as in-circuit test or flying probe machines, relies predominantly on having physical test access points. Many ATE machines now claim JTAG support, but some only use it to verify the existence of components that offer little or no access for conventional test probes.

Some vendors, however, are serious about interoperating with each other to produce an optimized set of tests that maximizes coverage while minimizing test time and fixture costs. This presents an opportunity for specialists in this field, to offer technology that produces high-speed, optimized tests, and some of the leading ATE and JTAG vendors can perform such optimizations.

Test Coverage

The purpose of any automated test or inspection equipment is to locate and,

if possible, identify manufacturing defects. Some defects could be design-related (e.g. the PCB may have been assembled correctly but the circuit's function is inherently wrong) but the EDA tools now available help ensure that a design can at least be tested as soon as the first prototype is manufactured.

Performing suitable design-time checks also saves engineers vast amounts of time writing custom functional tests at the board bring-up stage because full JTAG testing is available to diagnose issues much more quickly.

The extent to which a PCB can be tested for such defects, and therefore the effectiveness of any test equipment in finding those faults, can be measured. For any given PCB that figure will depend on the number of devices, the number of pins and the level of test access.

For ATE that relies on physical test access, the lack of test access points will lower that figure. JTAG can be and is used to significantly increase test coverage achieved by ATE, but it can also be used as a standalone alternative, addressing all of the recognized parameters for measuring and providing test coverage.

At the most basic level, JTAG testing can identify defects, such as open or short circuits on joints, but can also infer much more. With access to information, including BSDL files for the JTAG-enabled devices on the PCB, as well as (but not necessarily) the board's netlist and BOM, the software can determine the presence and correct orientation of components. The ability to access the chip registers of a device through JTAG-controlled components can allow confirmation that the right component has been fitted and that it is functioning.

It should be apparent that, even for a simple board, creating a test pattern to exercise accessible nets, interrogate devices on the board, and interpret the results is complex. Of course, understanding how the nets on a board are interconnected and optimizing the test pattern in response to that can significantly reduce the number of tests executed and therefore accelerate the overall test process.

This should be considered when evaluating the technology available from commercial vendors. While maximum theoretical test coverage is based on the board design and therefore beyond the control of JTAG test equipment vendors, the actual coverage attained and the ease with which tests can be created and executed is entirely under their control.

Most JTAG providers will loan their hardware and software equipment on a trial basis in order to allow engineers to assess it using their own boards, and draw their own conclusions. The best will even offer to do the board set up free of charge.

Functional Test and ISP

It is also well within the scope of commercial JTAG test software to develop functional tests for the active devices on a PCB, as well as use the functionality of non-JTAG devices to extend test coverage. This is normally achieved by writing tests which use the functionality of a device. These tests are often created by the JTAG equipment vendor and supplied in test libraries, although most tools also provide a way for creating custom tests.

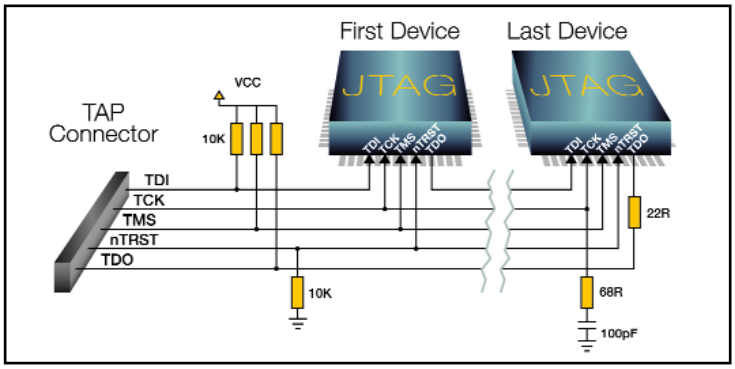

Diagram of good practice in JTAG chain implementation.

Another major use of JTAG is in-system programming (ISP). This uses the access provided by the JTAG interface to not only test, but also program devices on the board, often in a single process. ISP is also a feature supported by most FPGA vendors using their own software and hardware. However, commercial JTAG vendors are able to support ISP of almost any non-volatile device, as long as it is accessible from a JTAG-enabled device.

An example is XJFlash from XJTAG. It enables flash-based memories connected to FPGAs to be programmed in-system at much higher rates than with a conventional JTAG approach. It has also been extended recently to support the ISP of FPGAs with dual-ARM processor architectures, now available from multiple FPGA vendors.

Making JTAG Work

A JTAG interface comprises five signals, four of which are mandatory, collectively known as a test access point, or TAP. As the bus is daisy-chained between devices, the data out signal of one device becomes data in for the next in the chain. The TAP needs only one point of access to a board, typically through a small connector or header.

There are two critical aspects to getting successful implementation of the JTAG scan chain on a PCB: routing the TAP between devices, and maintaining the signal integrity of the TAP signals. Assistance can now be provided with both of these aspects. PCB designers using Altium Designer, Mentor Graphics PADS or Cadence's OrCAD Capture can now verify the scan chain from within the CAD tool. Plug-ins provided by JTAG vendors, such as XJTAG and JTAG Technologies, automate the process of verifying the scan chain.

This involves checking that the TAP signals are routed to the correct pins on all JTAG-enabled devices. The plug-ins can also display the level of test access that can be achieved using the respective vendors' tools. Designers can then take steps to ensure the TAP is routed and terminated correctly and that test access is maximized, during the schematic capture stage. This can greatly reduce the need for PCB re-spins.

In terms of maintaining signal integrity, XJTAG's plug-in can also verify that suitable pull and termination resistors have been added to the TAP signal nets. The plug-in also verifies that other pins which are needed to put JTAG devices into their test mode are not hardwired to the wrong values.

JTAG has been present in ICs for nearly three decades and shows no sign of being superseded by any other technology. In fact, it is evolving to ensure it will continue to meet the needs of designers and OEMs.

Currently, it can be used to check test access at the schematic stage, help debug prototypes, locate manufacturing defects, program non-volatile devices and even functionally test PCBs; in the future it will be used to embed virtual test equipment and improve support for testing differential signals.

It goes far beyond simply being a debug interface, and the work taking place within the IEEE ensures it will remain an active and progressive technology for years to come.

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