



DDR Memory Connectivity Testing and Boundary Scan

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With the complexity of electronic circuits continually growing and the increased use of BGA packages, ways to verify error-free assembly become ever more important. One option is boundary scan testing, which offers an automated method to check components are operational, correctly placed, and free from soldering faults, without the need to run any software on the board.

When JEDEC published standards for GDDR5 and DDR4 memories, they defined inbuilt test features that work with these systems to support rapid checking for assembly faults. Such methods can prevent many wasted hours by providing early detection of problems, and are as applicable to the first prototype boards as they are to mainline production.

The drive to support this style of in-circuit testing has continued into the latest GDDR6 specification, published at the end of 2018. Connectivity test methods are available for these memory devices, and similar checks can be performed on LPDDR4 and DDR3 components, which do not incorporate inbuilt test modes.

DDR4 Co

Larger DDR4 memories include a test feature that can be used to check the

connectivity of their pins. When the Test Enable (TEN) input is asserted, the memory cells become bypassed and the pins' functionality changes. Many become inputs, which an internal asynchronous

If a defect is found, a careful choice of input patterns even allows the fault to be pinpointed to a specific net.

The advantage of this method is that the test is performed without the

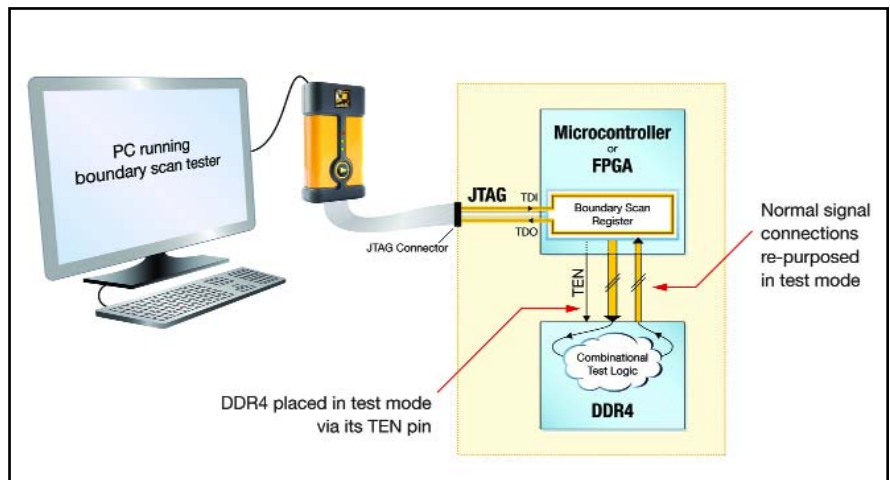


Figure 1: DDR4 connectivity testing.

logic tree combines to produce outputs on other pins.

By applying a series of different test patterns and reading the resultant outputs, it is possible to confirm that the non-power pins are free from open-circuit, short-circuit or "stuck-at" faults.

need to write or read the memory cells themselves, making it a fast process.

Gaining Access with JTAG

The simplest way for a PC application to apply these test sequences and to monitor the resulting outputs is to use

boundary scan techniques. This rarely requires any changes to the circuit board. In most designs, the DDR4 balls are already routed to a processor or FPGA that probably has boundary scan capability.

To initiate a connectivity test, a PC connected over the JTAG port places the processor or FPGA into JTAG test mode. This isolates its non-power pins from their normal functionality and instead connects them internally to a boundary scan register. This gives the PC control of the nets connected to those pins as shown in Figure 1. In this way, PC-based software can control the memory's TEN pin and apply the required test vectors.

The resulting outputs are read back into the register and then clocked serially out of the board's JTAG port for the PC software to analyze. This is all done without the need for any software to run on the board and is therefore suitable for early prototypes before any code has been written. All the low-level control is performed automatically by PC software that uses imported BOMs and netlists to make the process simple.

Practical Limitations

While this test mode was a welcome addition to the DDR specification, its approach of fixing which pins are inputs and which are outputs does impose limitations. For instance, the memory's DQS_t and DQS_c lines are used as two separate outputs in test mode. However, because they form a differential pair in normal use, the JTAG device's pins they connect to are often fixed in differential mode and therefore cannot be read as two independent logic inputs, even in boundary scan mode. This restriction, and the fact the feature is not mandatory on lower capacity DDR4 devices, has caused some users to be disappointed with this test mode. However we can look forward to seeing how it has been updated in JEDEC's long-awaited DDR5 specification.

GDDR5 Scan Test Mode

While GDDR5 (Graphics DDR, not DDR5) also includes a method for checking connectivity, it is different to that adopted in DDR4, because it does not use internal logic to combine inputs. When its Scan Enable (SEN) pin is asserted, its non-power pins are isolated from their normal functionality and are instead connected to an internal boundary scan register.

Test patterns are sent to that register over the device's parallel data bus and are applied to its pins. The actual states of those balls are then captured and serially clocked out of the memory's

"Scan Out" pin. At the same time, the JTAG device it connects to scans the other end of the tracks. Any differences between the sent pattern, the one read back, and what is seen at the JTAG device's end identify any connectivity errors. Repeating this with different patterns checks all the non-power pins.

As with DDR4, the memory chip is controlled for the duration of this test by the JTAG-enabled device to which it already interfaces. That device is placed

boundary scan registers using JTAG. The two memory channels have their own registers, with their individual data paths connected sequentially as shown in Figure 2.

As with all boundary scan techniques, when the memory is placed into test mode, its balls become isolated from their normal functionality and, instead, connect to the boundary scan registers shown in the diagram. A series of carefully selected test vectors are clocked

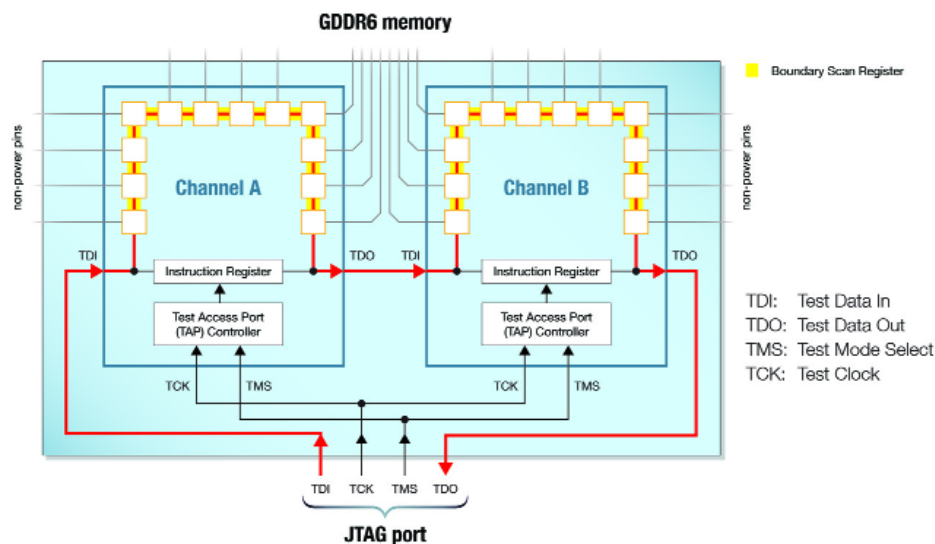


Figure 2: GDDR6 boundary scan.

into boundary scan mode, and the relevant bits of its boundary scan register become the control for the memory, the connection to the bus, and the input for the Scan Out data. Information is passed between the JTAG device and the PC using the board's test connector.

This test method imposes fewer restrictions than the DDR4 implementation because the four pins used to control the scan function are multiplexed onto signals that are defined as standard logic inputs in normal use (Scan Enable, Reset, Chip Select, and Mirror Function). It must be noted, though, that a circuit designer should not tie Scan Enable or Mirror Function solely to fixed voltages (a temptation for normal use) but should route them to pins of a JTAG device so that it can override their default state when in boundary scan mode.

GDDR6 Boundary Scan Test Mode

The GDDR6 standard brought IEEE 1149.1 compatible boundary scan to these devices. Unlike GDDR5, test patterns are not loaded by the data bus, but are serially clocked through the

into these registers with a JTAG connection, and the resulting states of the memory's pins plus those of other devices that can be accessed via JTAG are checked to ensure they are as expected. In this way, it is again possible to check for assembly faults on the memory connections, and to identify the affected net.

With GDDR6, it is not necessary to interface by using a JTAG device, but the JTAG can interface directly to the memory. Being a true boundary scan device, it can also be used to sample the state of all the nets it connects to, thereby checking continuity from other devices on the board. Due to its compatibility with IEEE 1149.1, a chain can be established that incorporates the board's processor or FPGA, the GDDR6 memory and any other JTAG-enabled components, simplifying testing of the complete board.

Testing LPDDR4 and DDR3

The method for testing devices such as LPDDR4 or DDR3 that do not have an inbuilt test feature entails exercising the address and data busses to write to the memory and then read it back. This is done by placing the JTAG device to which the memory is connected into boundary scan mode and using

that to manipulate the individual lines of the bus to mimic the read and write cycles normally used on the interface. In this way, test patterns are applied to the address and data busses and the memory's control pins.

Careful design of these test patterns makes it possible not only to detect an assembly defect, but also to identify the affected net. This test method is slower than using the built-in connectivity test features of DDR4 and GDDR5/6 memories because of the repeated memory read/write cycles required, but achieves identical test coverage.

Retention Time and Refresh

The memory's data retention time is relevant when discussing the use of boundary scan for DDR memory because the internal refresh cycles are not happening. The JEDEC standard specifies that DDR parts must have a retention time of at least 64 ms across its operating temperature range.

Writing a word into memory using boundary scan often requires twenty complete scans, and as it can typically take between 0.2 and 2 ms to perform one scan, we see that each write cycle generally requires 4 to 40 ms. A complete test can therefore exceed 64 ms. However, devices in practice have retention times far in excess of that specification limit, and studies have shown that even the leakiest cells have data reten-

tion of over a second at room temperature — perfectly sufficient for boundary scan requirements.

High-Speed Testing

In comparison to the speed at which DDR runs, boundary scan testing can be considered DC. This has an advantage in that it can detect micro-cracks in the solder joints that high-speed tests may miss due to capacitive effects enabling a high-frequency signal to pass where DC cannot. Such cracks can lead to early-life failures when they experience thermal expansion/contraction and oxidation.

As well as running a boundary scan, however, it can be beneficial to perform a high-speed test because signals may behave differently when running at MHz rates. A simple way to achieve this is to load test firmware into the processor or FPGA that interfaces to the memory to allow it to perform the write/read cycles directly, rather than going through boundary scan registers. Test patterns will now be loaded and read at high speed over the normal busses, executing a high-speed test. The disadvantage of this is the need to write processor-specific software, whereas the boundary scan test has no such requirement.

Although DDR4 DIMMs may be built from memories that have ten control inputs, those signals are not routed to the connector. When performing automated tests on assemblies using DIMMs, the

DDR4 connectivity test mode cannot be used. In that instance, it is necessary to use standard boundary scan test methods, such as those described for DDR3.

We have seen that the current generation of memory devices, such as DDR4 and GDDR6, incorporate internal circuitry that provides fast and efficient methods to confirm the part has been correctly placed on the board, that it is functioning, and has no soldering defects such as open-circuit, short-circuit or "stuck-at" faults.

These connectivity test modes have led to a reduction in the time taken to check the devices because there is no longer a need to write and read to the memory cells during testing. When designing a board that incorporates memories with an internal test capability, it is strongly recommended that Test/Scan Enable and other control signals are routed to the I/O pins of a JTAG-enabled component or to a test header. By doing so, the designer enables the use of automated connectivity testing that can save many hours of debug time on first prototypes, as well as during mass production.

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