*Reprinted with permission from the August 2010 issue of ...*


# Test and Measurement Reaches for Debug

**By Simon Payne, CEO, XJTAG, Cambridge, UK**

Reducing test cycle time while increasing test coverage is an important goal for equipment builders serving all types of markets, including military, aerospace, and transportation.

As far as military equipment is concerned, manufacturers are turning to advanced networking technologies to enable them to configure, coordinate and extend their capabilities cost-effectively — including integrating new and smarter equipment. Advanced networking and communication technologies allow new functions to be added quickly as services on the net, but also drive equipment developers to seek the most advanced components such as field-programmable gate arrays (FPGAs), advanced processors and high-performance standard ICs.

***Boundary scan equipment provides tools for fast, high-coverage test solution for mission-critical PC boards.***

These components typically incorporate leading-edge package styles such as ball grid array (BGA) or flip-chip packages with underside-mounted I/Os that are not physically accessible, making units difficult to test using laboratory test gear, bed-of-nails test fixture, or field-based equipment.

As the use of devices in advanced packages continues to increase, the test coverage that can be achieved using typical probe-based test techniques is reduced. Engineering teams need an improved test solution that will overcome this challenge while also reducing the time to debug prototype boards, helping to pinpoint production defects rapidly, and aiding diagnostics and repair of units returned from the field.

Many high-performance components on the market today are JTAG-compatible devices which have built-in boundary scan circuitry. Boundary scan provides a convenient way to test devices without requiring physical access to probe each pin. As the number of boundary scan components on successive new board designs increases, so, too does the level of test coverage that can be achieved by applying boundary scan tests. The latest boundary scan test equipment, combined with careful use of best design practice, can increase test coverage further still. Many companies, including well-known defense contractors, have achieved over 80 percent test coverage for some boards using boundary scan alone.

### JTAG Finally Comes of Age

Boundary scan testing was originally proposed by the Joint Test Action Group (JTAG) as far back as the 1980s, and is covered by the IEEE 1149.x standards. The underlying standard defines a test access port and boundary scan architecture, implemented in the silicon of the device to be tested. The circuitry behaves like a general-purpose serial communication port, allowing values to be read into and out of the internal registers, memories and gates of devices such as processors, FPGAs, and memory chips.

The test ports of all such devices in the system are interconnected at the board level. This creates a serial data path, or boundary scan chain, that can be accessed via a single edge connector. By shifting calculated sequences of data into the registers of target devices, and monitoring the returned results, boundary scan test equipment can verify that the components are connected correctly and functioning as required. Test patterns can be shifted into and out of a unit under test without needing to boot up the board. By manipulating the scan chain to set up suitable test patterns, responses can also be collected from components that do not offer a boundary scan test interface, provided the device is connected to the same net as a compliant device. This technique is sometimes referred to as “cluster testing”, and provides a way of testing non-JTAG devices such as external connectors, video chips, IIC devices, Ethernet controllers, LEDs and switches. Hence, as the numbers of boundary scan devices per board increases, the total

test coverage achievable using boundary scan increases even more quickly.

**Advantages for Users**

Boundary scan testing is being adopted quickly by companies such as defense electronics businesses, as pressure on test access and time-to-market continue to intensify. Today's boundary scan test equipment, such as the XJTAG development system, uses highly evolved software that calculates how to manipulate the boundary scan chain to achieve the maximum possible test coverage, while providing an accessible, easy-to-use GUI. This not only improves testability compared to traditional probe-based methods, but also reduces the time engineers typically spend developing tests and applying those tests to prototype or production boards.

Thales UK, has used XJTAG to test FPGA-based boards for a Software-Defined Radio (SDR) platform, this radio is designed for naval and ground-based applications and will be used on the Royal Navy's Type 45 Destroyers. "We were up and running within half a day," says Gary Delamere, a senior engineer at Thales UK. "Test coverage, for digital circuits, is up around the 80 percent mark already."

Curtiss-Wright Controls is another important international defense business utilizing boundary scan to overcome the test challenges presented by complex, high-value communications boards. Stuart Allen, senior hardware engineer at Curtiss-Wright's video and graphics group, comments, "Using XJTAG, we are able to very quickly debug and test both the boundary scan and cluster devices on our Sabre and Osiris boards, many of which are inaccessible to traditional test methods such as flying probes, logic analyzers, oscilloscopes and X-ray systems."

The military and aerospace sector is not the only market for high-reliability equipment where boundary scan testing is gaining a large following. Westinghouse Rail Systems is one of the world's foremost developers of advanced integrated signaling and control systems for main line and mass transit railways. The company is using the XJTAG Professional boundary scan system to support rigorous testing of advanced prototype hardware designs using the latest component package technologies, and to increase flexibility as well as reducing design-to-completion times for complex projects. As R&D hardware engineer Jeff Smith explains, "XJTAG has a powerful range of functions that allow us, to control devices from the inside and regain visibility of all the hidden BGA interconnects in the JTAG chain. We can also read or write pins and busses with a single click using XJAnalyser."

**Use it from the Start**

By using boundary scan from the beginning of each design project, for tasks such as validating CAD netlists, Westinghouse has successfully reduced the time and cost to develop and prototype its boards. The latest generations of boundary scan test systems provide graphical tools that help engineers visualize their boards and develop sophisticated boundary scan tests very quickly. In addition, high-level test-description languages such as XJTAG's XJEase allow custom tests to be written quickly and easily.

Because boards do not have to be running before performing boundary scan tests, development engineers can quickly verify basic functionality as soon as first prototypes return from assembly, without first having to debug the processor or memory system. Moreover, development engineers who use boundary scan report that this approach is more predictable and usually faster than "buzzing out" prototype boards, which often takes several hours or even days. Thales, in fact, saved around 20 percent of the time normally spent testing and debugging boards, when using XJTAG boundary scan to develop its SDR platform.

**Building Test IP**

As the use of devices in advanced packages continues to increase, the test coverage that can be achieved using typical probe-based test techniques is reduced.Importantly, the increasing power of boundary scan test equipment allows development engineers and production test engineers to adopt a common toolset and to share and re-use tests. This can potentially save much of the time ordinarily spent devising tests for certain modes or faults on production models, after development teams have already devoted time to solving similar challenges during prototype and debugging stages. The act of writing a boundary scan test as a script can be viewed as creating test IP; this is then available to be re-used later in the project, when developing tests for use on the production line, or to help with diagnostics and repair of units in the field.

**Development engineers who use boundary scan report that this approach is more predictable and usually faster than "buzzing out" prototype boards.**

QSI Corporation, Salt Lake City, Utah, designs and manufactures rugged Human Machine Interface (HMI) modules and Mobile Data Terminals (MDT) for industrial OEMs and commercial vehicle systems integrators. The company has integrated boundary scan into the production-test stations it provides for its manufacturing partner to test production units.

The terminals are designed to withstand high levels of shock, vibration, humidity and other environmental conditions. In the event that a unit is returned for repair, probing every data, address and control line to locate the cause of a field failure can take one to two hours. According to Eric Anderson, an electrical test engineer at QSI, boundary scan now allows service engineers to collect the data they need within around 15 minutes.

The experiences of world-leading companies goes to show how boundary scan can solve important test challenges throughout prototype and debug, test and measurement and service and repair roles and in the process save time and money.

*Contact:* XJTAG, Dirac House, St. John's Innovation Centre, Cowley Road, Cambridge CB4 0WS UK
☎ +44 (0)1223 223007 fax: +44 (0)1223 223009
E-mail: simon.payne@xjtag.com
Web: www.xjtag.com ❒