

Signal Integrity in Test Fixtures

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Stable and reliable test procedures are important to avoid unnecessary, and sometimes costly, delays in production. When these require some form of test fixture connecting a device under test (DUT) to the automatic test equipment (ATE), poor signal integrity between the two can often make tests unreliable. Identifying and resolving such problems can be time consuming, but by following some simple guidelines when designing both the DUT and fixture, test stability can be significantly improved.

JTAG Test Access Port (TAP) signals, used to implement boundary scan testing, will be used as an example, although other test and programming protocols can also benefit by following these guidelines.

Minimising the Loop Area

When signals are connected within a test fixture it is quite common for the wires carrying those signals to be given far more consideration

than the return ground connection. A ground is likely to be included somewhere, but could it be improved?

With low-frequency and DC signals, the routing of ground wires relative to the signal wires can be different without any obvious side effects. However, as the frequency of the signals increases, the routing of the ground wires becomes more and more significant, up to the point where getting matched impedances is important. For TAP signals, such levels of precision are often not necessary; however minimising the loop area is a good rule of thumb.

The key to identifying the loop area is to determine:

1. The route that a signal's current will take from its source to destination. This is often easy to establish, because it is the same route as the signal's wires and tracks.
2. The route that a signal's associated return (ground) current will take from the destination back to the source. This can be slightly harder to establish, but can be approximated by assuming it stays as close to the signal as possible.

It is important to realise that this doesn't just cover the cables between circuit boards, but also the route of the current around each board.

To minimise the loop area, the physical area bounded by the signal and its return current should be minimised. Ideally the signal and its return will be routed directly next to one another, which can be easily achieved in a ribbon cable (Figure 1a) or a traditional twisted pair (Figure 1b). Both of these arrangements have small loop areas, and so will help improve signal quality.

As soon as the return path for the ground current takes a different route to the signal current then a much larger loop area is formed causing three problems:

1. The signal becomes much more susceptible to electromagnetic interference (EMI)—the cable becomes an aerial picking up electrical noise.
2. The signal is radiated away from the cable, creating additional electrical noise that may interfere with other signals.
3. There is a change in characteristic impedance as the signal propagates down the cable. This degrades the quality of the signal.

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Figure 1c shows an obvious case where there is a larger loop area, and demonstrates how easily this can occur if care is not taken to keep the signal and return wires close together.

How to Minimise the Loop Area for Test Fixtures

Test fixtures are often created using many individual wires, one for each active signal. Although this makes it easier to wire up the fixture, it can also lead to an electrically noisy environment and consequently signal integrity problems which are particularly evident when using JTAG.

Figure 2 shows some common mistakes seen in test fixture design: The ground connection to the JTAG controller is connected to the DUT a long way away from the TAP signal connections; and the ground and TAP signal cables do not run close to each other. This can be easily,

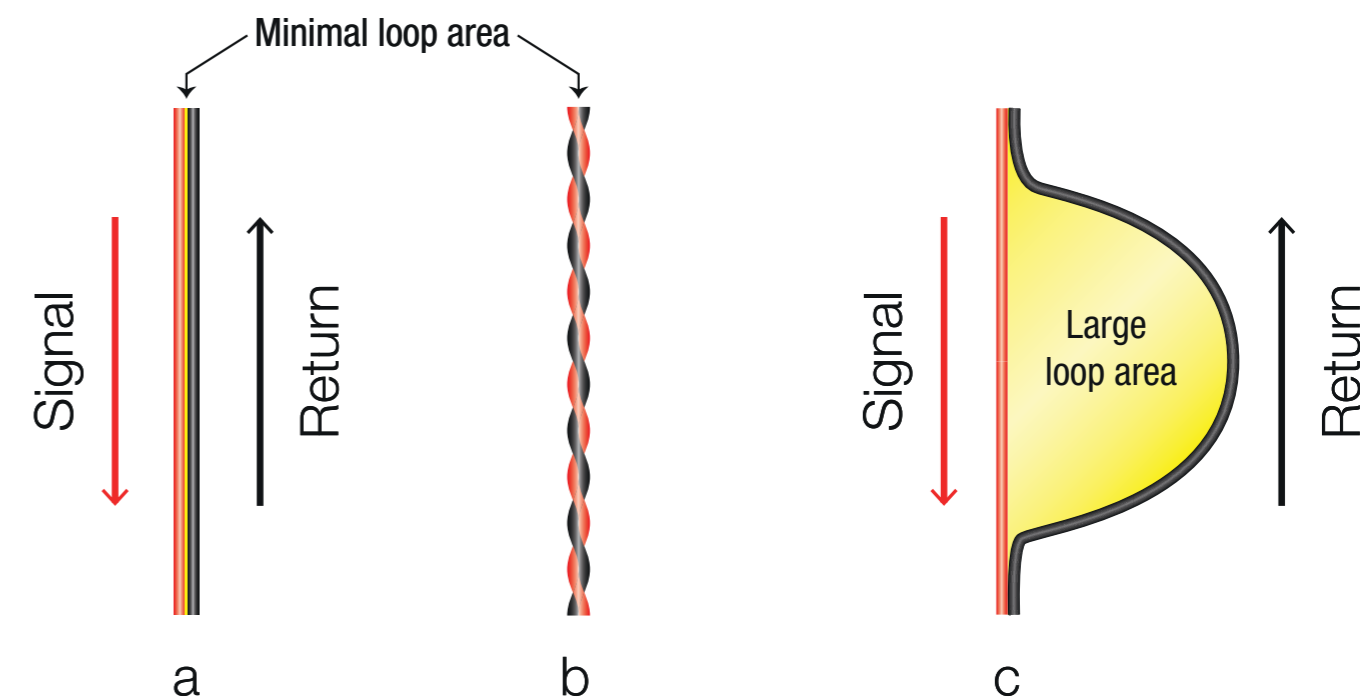


Figure 1: The arrangement of signal and return cables using (a) ribbon cables, (b) twisted pairs, and (c) individual wires, can have a significant impact on a signal's loop area.

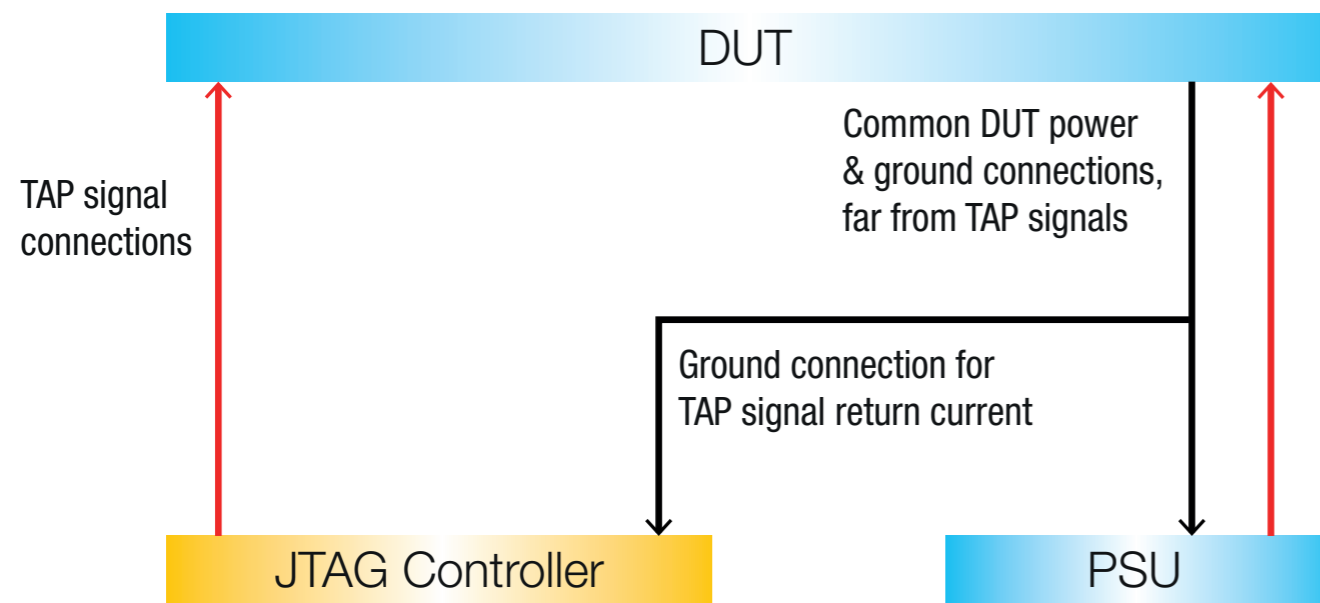


Figure 2: A bad test fixture design, due to large loop areas for all TAP signal connections.

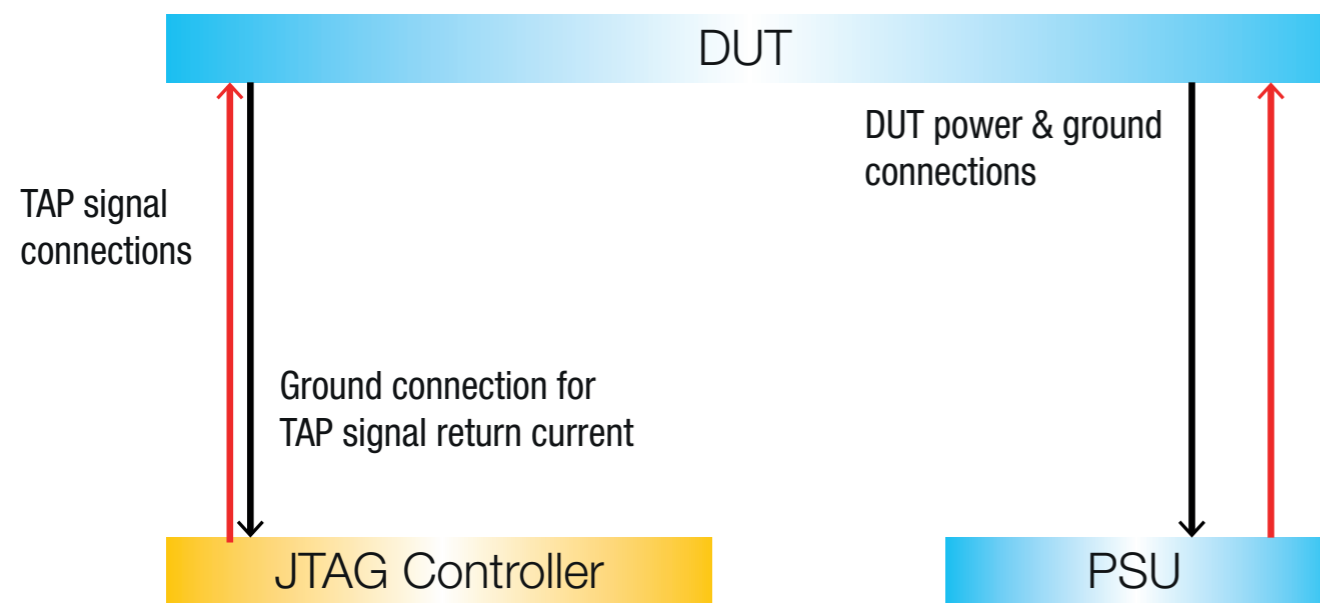


Figure 3: A good test fixture design, keeping the loop area small for all TAP signal connections.

and significantly, improved by making the following changes, as shown in Figure 3:

1. Add at least one ground test pin as close as possible to the TAP signal test pins in the test fixture. This isn't for the main ground connection used to power the board, but instead is to

provide a good ground connection between the JTAG Controller and the board to improve the signal quality.

2. Use twisted or parallel pairs, each containing one signal and a ground, for each TAP signal. This is most important for the clock signal (TCK) but also any other signals that are

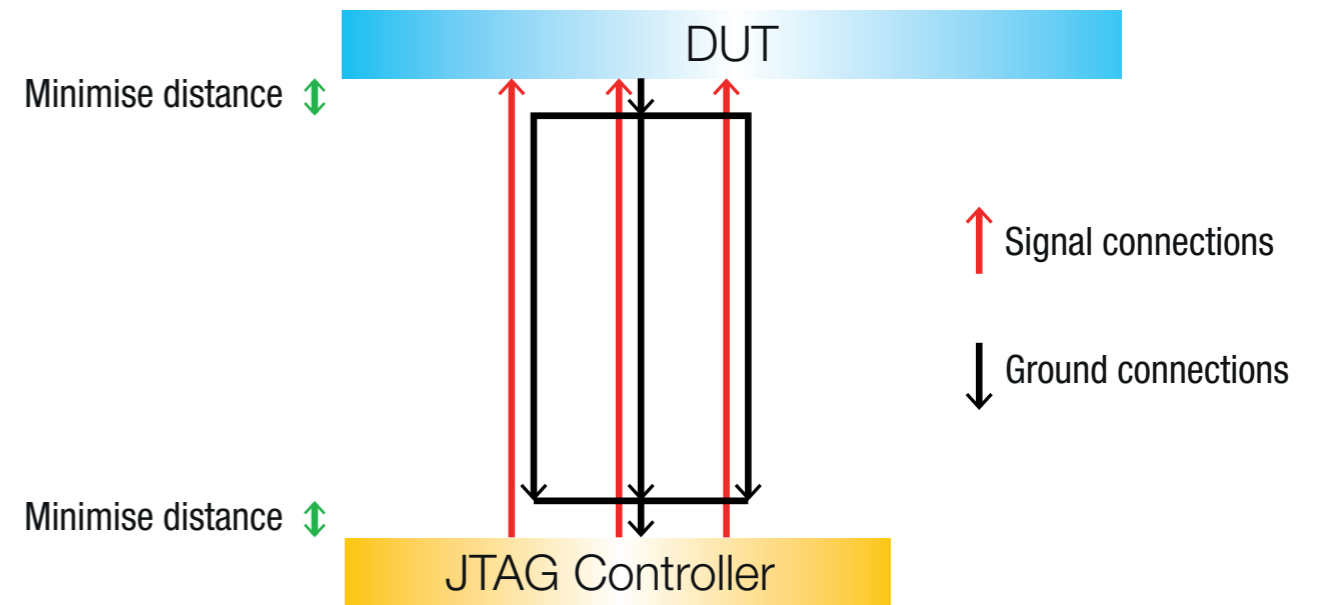


Figure 4: Wiring multiple signals when there are not enough ground connections on the DUT or JTAG controller.

continuously switching (i.e., TMS, TDI and TDO). When the JTAG Controller has fixed (hard) ground pins as well as configurable (soft) ground pins, a minimum of at least one hard ground connection should be used.

There does not need to be a separate ground test pin for each signal/ground pair, and instead the ground cores in multiple pairs can be connected to the same test pin. If this is not directly possible then small adapter boards can be used to share one ground connection across multiple pairs. No matter how this is achieved, it is important to keep the ground and signal wires close to each other, as shown in Figure 4.

When using connectors directly on the DUT instead of test pins, a similar philosophy can still be used. For example, separating signals in a ribbon cable so they are interleaved with ground connections is sensible whenever possible, and the importance of doing this increases as the length of cables increase. If the DUT connectors are not designed to allow this organisation then it can be achieved by creating a custom cable. This might appear to be making things more complicated than they need to be; however, as previously stated, getting this right early on can significantly reduce

the cost of fault finding later on during test development.

Minimising the Loop Area for PCB Design

To help ensure a PCB can be thoroughly and reliably tested, its testability should be considered during the design phase and not just considered as an afterthought. Design for Testability (DFT) guidelines can cover a wide range of areas, many of which focus on improving how much of a PCB can be tested. However, if the signals used to implement this testing are not considered, it is possible to design a board that can be thoroughly tested but where the tests themselves are unreliable.

Improvements to a PCB design can be split into two categories: improving signal connections to the board, and improving the signal routing within the board. The first of these should allow a test fixture to be created that can easily minimise the loop area:

- When using test pins include one ground test point close to each TAP signal test point. If board space is limited, try to include at least one ground test point for each pair of TAP signals.
- When using headers that will be connected via ribbon cable, include ground pins

so that there is one ground core between each TAP signal in the ribbon cable. If the number of available pins is limited, as a minimum try to include ground cores on both sides of clock signals, such as TCK.

Even with a well designed test fixture and good test signal connections to the DUT, it is still possible to make JTAG tests unreliable if a PCB is not designed correctly. Leaving the routing of the TAP signals until last might initially appear to be sensible: They're only for testing the board, so why not route all functional signals first? The problem is that this can result in poorly routed signals that can make the testing unreliable, and in the worst case can even require a new board design, resulting in significant extra expense and delay.

It is worth keeping in mind that TAP signals can clock at frequencies exceeding 20 MHz. This means they should be treated just like any other signals at similar frequencies:

- Correct signal termination should be applied to the signals, as specified in JTAG DFT guidelines. These follow standard good design practices, such as placing parallel termination resistors as near to the receiver end of a track as possible.
- Avoid stubs in tracks, and use buffers to improve signal fan-out.

- Route TAP signals over a continuous ground or power plane. If there are breaks in this then the loop area is increased, making the board more susceptible to unreliability during test.

Figure 5a demonstrates how the routing of a TAP signal trace (red) across a break in a ground plane can affect the return current path (black dash). This results in a larger loop area than initially expected, deteriorating the signal integrity. Although the signal track is longer in Figure 5b, the total loop area is still reduced and so this would be the preferred solution if the ground plane could not be changed.

Summary

Minimising the loop area will always be a rule of thumb, and as such is not always applicable. However, by being more aware of the route a signal's return current will take, this can provide a solid foundation when designing PCBs, determining the pin-outs for connectors, and designing and building test fixtures. By considering this as part of the design process, costly and time-consuming delays later in the development cycle can be avoided. Where available, DFT guidelines should also be consulted, because these will contain additional information to further improve the testability of DUTs and the reliability of these tests.

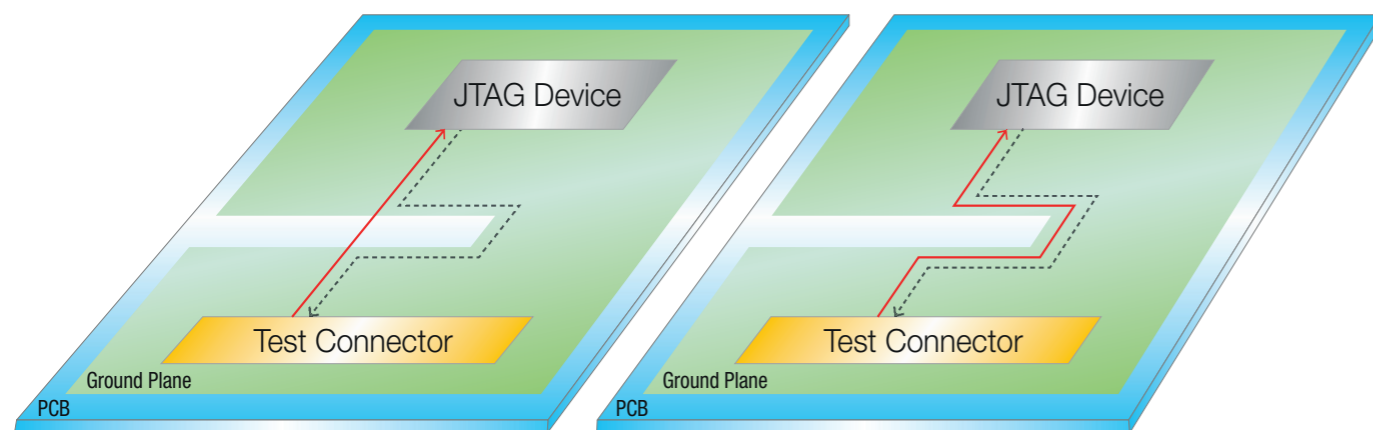


Figure 5: Return current through a ground plane (black, dashed) will follow the signal trace on a different layer (red) where possible. Routing over breaks in the ground plane (a) can significantly increase the loop area, and so should be avoided (b).

What is boundary scan?

JTAG boundary scan is an electrical test method designed to overcome problems in test access generally associated with complex, high density boards. Components such as FPGAs, CPLDs and CPUs contain boundary scan technology, which allows engineers to stimulate and test the circuitry digitally with a JTAG Controller and attached software, in order to pinpoint precise locations and causes of faults.

Boundary scan reduces the requirement for test points on the circuit board, so the physical access problems associated with ICT and some functional tests are no longer an issue. The test system and boundary scan cells are connected only by means of a four or five-wire test bus, which must be considered during board design to ensure testability. Many leading vendors of JTAG boundary scan systems supply DFT guidelines to encourage design engineers to do so.

How does it work?

All the signals between a boundary scan compliant device's core logic and its pins are intercepted by a serial scan path known as the boundary scan register (BSR). In normal operation these boundary scan cells have no effect; however, in test mode the cells can be used to set and/or read values from the device pins. A set of four or five JTAG Test Access Port (TAP) signals are used by boundary scan enabled devices to allow the boundary scan data to be transferred to and from the device, allowing controlling software to analyse the circuit's performance. **SMT**



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