Getting it right at the design stage

Design engineers can now leverage XJTAG's experience to maximise the power of boundary scan in their designs. By **Graham Pitcher**

Like the technologies which sit upon them, printed circuit boards are getting smaller. While that has a positive outcome in terms of smaller products, there is a negative aspect. Increased component densities mean access to the pins on chips or the balls beneath them has become almost impossible. The 'good old days' of being able to attach probes to the pins emerging from a package have long since gone.

For the last few years, this has been more of a concern for those performing manufacturing or prototype test. A solution has been the development of so called boundary scan techniques, developed by the Joint Test Action Group (JTAG) and codified as IEEE1149 in the early 1990s. By creating a scan chain, the performance of many components on a PCB could be verified, as could the quality or otherwise of the solder connections. Inherent in the success of the JTAG scan chain is getting it right at the design stage.

According to Simon Payne, XJTAG's CEO: "JTAG can do more than just provide test access; it can also be used for processor debug/emulation and programming.

"JTAG is implemented in CPUs, programmable devices and the other ICs that typically form the heart of any electronic product; however, its potential is often overlooked. Until now, design tools didn't include any way to verify the JTAG system at the design stage."

Yet, despite the fact that JTAG has been around for many years – and XJTAG has been developing boundary scan based test products since 2003 – engineers are still finding problems because they make simple errors in their PCB designs. And XJTAG says these errors are avoidable.

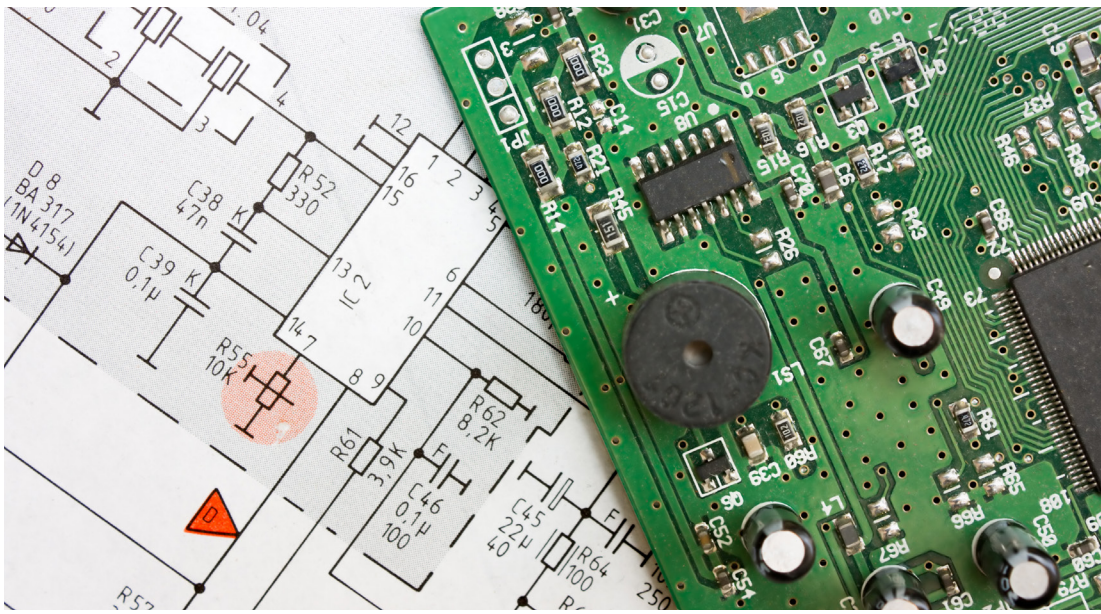

Image: Adobestock

Its solution is the XJTAG DFT Assistant, which it describes as a new tool that enables the early correction of design for test errors in PCB layouts. "For the first time," Payne said, "engineering can validate proactively the test access to their designs from within their CAD application and before any hardware is produced, preventing costly respins and delays."

So how was the need for DFT Assistant determined? He pointed out that XJTAG's team interacts regularly with the design community. "In most situations, we only encounter designs at a point where it is already too late to fix any design problems without the client needing to respin the board.

"Seeing such a wide range of boards with varying quality of JTAG implementation gave insight into the needs of the electronics industry. It became obvious that none of the PCB design tools offered a way for PCB designers to check their JTAG implementation was connected and terminated correctly. This realisation resulted in the proposition of using some of XJTAG's IP to provide a helpful extension plug in to the design tools, showing at the design stage the available test access to a PCB," Payne explained.

What's different about DFT

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Simon Payne

Above: The XJTAG DFT Assistant provides powerful testability analysis

Assistant is that has been made available as an extension to PCB design packages from four leading vendors – Altium, Cadence, Mentor Graphics and Zuken. Introduced in 2016, DFT Assistant has been made available free of charge, minimising the barriers to adoption.

"We saw that our customers could benefit from direct integration of JTAG in OrCAD Capture," said Kishore Karnane, director of product management with Cadence OrCAD Solutions. "XJTAG was the ideal partner to help us achieve this, bringing its specialist knowledge and expertise in testability issues and design."

The collaboration has resulted in XJTAG DFT Assistant for OrCAD Capture; a two part solution consisting of the XJTAG Chain Checker and the XJTAG Access Viewer. XJTAG Chain Checker is intended to identify common design issues, such as connection errors in the JTAG chain design or incorrect termination of signals at Test Access Ports. XJTAG Access Viewer, meanwhile, is designed to help the testability of designs to be assessed and to identify where coverage could be improved.

The extent of JTAG access is displayed as an overlay on the schematic diagram and a selection tool enables engineers to analyse specific areas of interest by displaying the test access to nets – read, write, power/ground or no access – individually or in groups using checkboxes. Nets are colour coded by JTAG access to aid inspection.

Karnane added: "XJTAG DFT Assistant enables us to deliver greater value for our customers by providing powerful testability analysis."

Altium also saw the benefits of adding boundary scan chain verification to Altium Designer, its platform that supports the addition of supplemental functionality through approved third party extensions.

"By collaborating with XJTAG, we've been able to expand the value of the Altium Designer platform for our customers with the first-ever extension to verify boundary scan chain design and ensure DFT best practices are achieved," said Daniel Fernsebner, Altium's corporate director, technology partnerships and business development.

Mentor Graphics is another collaborator. "Boundary scan can add value from the beginning of the product lifecycle, and is becoming increasingly important to our customers," Jim Martens, product marketing manager with Mentor's PADS Solutions Group, noted. "We saw the opportunity to enhance PADS by integrating the features of XJTAG's DFT Assistant.

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Jim Martens

"Our customers can now use PADS to produce even better board designs that benefit from higher test coverage, faster debugging and prototyping, and more efficient testing in production."

Payne said the aim of releasing XJTAG DFT Assistant was to provide a tool to increase the number of board designs which could be testable, programmable or debuggable using JTAG. "The first objective was to collaborate with all of the leading PCB design tool providers in order to allow as many engineers as possible to benefit from the tool – this has been achieved.

"The second objective," he added, "was to educate the market about the advantages of designing early for testability and the cost and time savings that can be achieved – this is ongoing."

"The importance of this product, as the take-up shows, is that JTAG is moving from manufacturing into mainstream design and was a fundamental piece of the jigsaw missing until now. Engineers are not necessarily aware of how to design JTAG to give good signal integrity and this product allows engineers who are not experienced with JTAG to achieve a working design at their first attempt."