The chain gang

Boundary scan test is a must for designers using fpgas and cplds. By **Dominic Plunkett**.

Reconfigurable components such as fpgas give engineers greater flexibility to update designs quickly and to deliver new products to an aggressive roadmap. But there can be untested hardware faults in circuitry that is not used until the upgrade is applied. Engineers need fast and effective techniques to test this dormant hardware.

With the prices of fpgas, cplds and mcus falling, it is becoming common for engineers to implement new features by reprogramming existing hardware or by updating software, bypassing the redesign of fundamental hardware. Upgrading by reprogramming also allows engineers to respond quickly to emerging standards, as is common in mobile communications. It can also ease customisation of designs to meet individual customer requirements.

Latent faults

Designing a product with upgrading in mind maximises the economies available from reprogramming. However, the first generation fpga design will typically leave a number of I/Os and internal functional blocks unused. It is also common for certain mcu peripherals or ports, such as counters or uarts, to be left for use by later software releases. In practice, these unused parts of the hardware are unlikely to be tested in the first release. It is always difficult to verify that a set of tests will exercise 100% of functions and modes, but the task becomes impossible when some of these have not yet been determined.

For units that are designed for field upgrade, this can be a problem. Hardware faults not identified by the original production tests may surface when the newly increased functionality is exercised, leading to additional engineering and replacement costs. But undiscovered faults can also slow development when a second generation design is being prepared in house.

The need to go back and correct a deep seated design flaw introduced at an earlier stage will delay the project timetable and increase the engineering costs. Some of these faults may be as trivial as a routing error, or could be process related such as persistent poor solderability of a component. By identifying these issues in the first generation of the product, engineers can rectify basic errors and save time when developing future generations of products based on the same hardware.

With the largest fpgas featuring thousands of I/Os per chip, extensive physical testing of interconnects is impractical. Moreover since most medium to large fpgas, as well as mcus, are supplied as bgas, physical access to I/Os is usually not possible. Traces between ics are also frequently inaccessible, existing several layers beneath the surface of the pcb.

Boundary scan

Boundary scan testing offers a solution to the problems of unearthing faults in untested connections and features of programmable components. A boundary scan test detects automatically hardware faults associated with devices included in the scan chain. All device pins – even those in physically inaccessible locations – can be exercised and inspected for faults, including opens, shorts and stuck at conditions.

To be testable using boundary scan, a

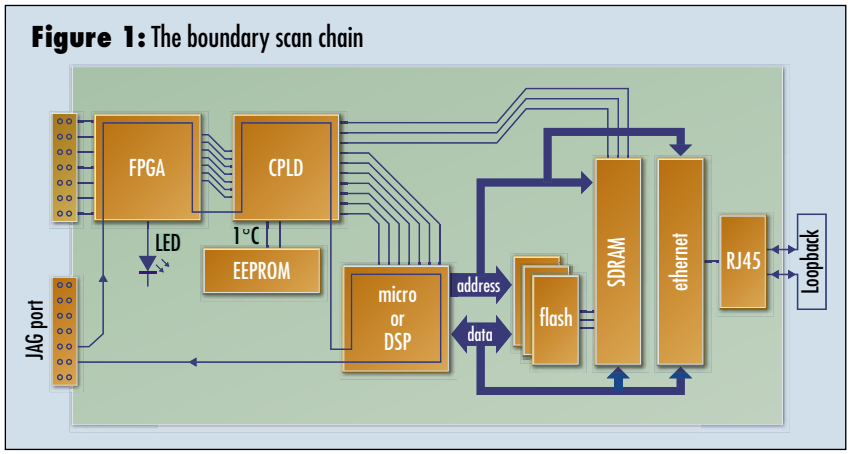

Figure 1: The boundary scan chain

device must implement a test access port and boundary scan circuitry comprising shift registers and a state machine to execute boundary scan functions. A sequence of test bits is clocked serially through the device to stimulate the device core, drive and sense device outputs, and sense inputs. Manipulating the test sequence exercises specific device functions, while the returned data contains information about the operation of the device and the hardware connections to its pins. Fortunately, there are boundary scan compliant versions of most fpgas, cplds and microcontrollers.

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Dominic Plunkett, **XJTAG**

To apply boundary scan testing at the board level, a boundary scan chain must be implemented to physically link the JTAG compliant devices on the board, as shown in figure 1. Designing the scan chain is relatively easy, involving serial linking of the In (TDI) and Out (TDO) pins of the boundary scan ports, as well as routing of the boundary scan clock to each ic in the chain.

However, mistakes can be made. Common errors include incorrect linking of TDI and TDO pins, as well as general routing errors that may result in an incomplete or incorrectly routed scan chain. For this reason, designers must apply the same care when designing and implementing the scan chain as with any other part of the board layout. Good physical access should also be provided to the chain itself, to allow probing for rapid identification of any errors. Also, even though typical clock frequencies for boundary scan testing are relatively low, the scan chain should also be kept as short as possible to ensure optimum signal integrity and glitch free clocking.

The latest boundary scan test tools, such as XJTAG, present a graphical, real time display to allow engineers to visualise the status of each interconnect on a host pc. Any pin can be toggled and specific values written to and read from groups of pins that the engineer can define as a bus for the purposes of a test. In practice, engineers can quickly establish a high level of test coverage via the boundary scan chain. It is also possible to write values to other devices connected to the boundary scan chain, including those that do not have boundary scan circuitry integrated, and read the returned values to increase test coverage still further.

Boundary scan testing is a valuable technique for development engineers, who can begin testing as soon as the first hardware is ready. Basic functions can be tested without booting up the board or running software. Importantly, this approach to testing at the prototype stage records automatically the tests that are applied to the board, unlike more traditional test and debugging techniques. Successful tests can then be carried forward to provide a head start for production test development, taking advantage of boundary scan to exercise inaccessible nets and reprogrammable devices in production units.

In this way, boundary scan can break down the wall that usually exists between prototyping and production. By working together to review existing tests from the prototype phase, development and production test engineers can reduce time to market by eliminating much of the duplication of effort inherent in a conventional test engineering approach.

Building on the tests available from the prototype phase, production test development can then add extra boundary scan tests to meet test coverage targets for production units, frequently in combination with functional test and in circuit test routines. These enhanced tests can then be reused for the next prototype.

By applying boundary scan testing in both the prototyping and production phases, the resulting continuity not only streamlines time to market for the current product but also benefits development of the next generation.

As an evolution of its predecessor, the subsequent design can benefit from production quality tests from the earliest stages of prototyping. As the development creates new tests to exercise the revised features, these then become valuable to subsequent production test engineering.

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