Military sets sights on JTAG to meet test coverage challenges imposed by COTS design

By Dominic Plunkett

The increasing deployment of FPGAs and other JTAG-enabled ICs across aerospace and defense products is forcing board designers to think again about boundary scan/JTAG test solutions.

Designers of military electronic systems are under intense commercial pressure to deliver advanced systems on time and on budget. Using leading-edge COTS semiconductor components is an effective way to achieve very high performance targets within tight time constraints, particularly for network-centric and C4ISR systems.

However, the prevalence of fine-pitch and Ball Grid Array (BGA) package styles among COTS devices restricts physical access to connect test probes during development and in production. This can hamper development work and may also prevent test engineers from achieving the levels of test coverage stipulated in the product or board specification.

Since modern boards afford negligible real estate for dedicated test access points, an alternative test technology is required that does not rely on extensive physical access to the board. Boundary scan or JTAG testing, as described in the IEEE1149.1 standard, offers a solution.

Boundary scan testing

The techniques for boundary scan testing were developed by the Joint Test Action Group (JTAG) and ratified by the IEEE in 1990. Test access was already under threat, but today's surface mount packages add an even greater sense of urgency. It appears that JTAG's time has come – an impression reinforced by the growing number of JTAG-compliant ICs now entering the market.

FPGA vendors are notable for offering a large number of JTAG-compliant components. Since these devices, such as the FPGA shown in Figure 1, can have more than 1,000 I/Os, it is not too surprising that board and test designers are turning to boundary scan testing in preference to alternatives that require physical probe access.

Testable, custom military silicon

With increasing use of military-qualified, JTAG-compliant devices, JTAG test gear can be used to test military boards even more extensively as the number of such nets continues to rise. Early collaboration between military chip designers and production test engineers can improve this situation still further.

Figure 1

For example, designers of Application Specific Integrated Circuits (ASICs) for military projects can directly influence test coverage for the better by designing JTAG circuitry into the silicon from the outset. This will significantly ease the task of ensuring the board reaches its testability targets. Military designers also have greater freedom than their commercial counterparts to implement JTAG circuitry on-chip because low production volumes and the high value of each component mean there is less price pressure to minimize die area.

About boundary scan testing

The IEEE 1149.1 standard defines a standard test access port and boundary scan architecture comprising shift registers and a state machine to execute boundary scan functions, which must be implemented in the silicon of a complex IC.

This circuitry allows a sequence of test bits to be clocked serially through the device. The test sequence can be designed to stimulate the device core, drive and sense device outputs, and sense inputs. The Printed Circuit Board (PCB) must be designed to connect multiple ICs via this integrated boundary scan logic, thereby setting up a serial scan chain that supports electrical access to all pins on each IC included in the chain. Hence, boundary scan testing must be considered early in the design cycle, as part of a Design For Test strategy. When the board is functioning normally, the boundary scan circuitry is disabled.

Connection testing and In System Programming (ISP) are the two applications most commonly associated with boundary scan. However, by using the interconnecting nets between the devices in the JTAG chain and other devices in the circuit, it is also possible to access non-JTAG-compliant sections of a circuit using boundary scan. This significantly extends technology power by allowing a greater proportion of each board to be tested, thereby increasing test coverage without requiring physical access to individual pins. With more JTAG-compliant devices on the PCB, the number of noncompliant devices that can be accessed using the boundary scan chain also increases.

With growing rates of JTAG compliance among COTS and custom ICs, boundary scan testing has the potential to deliver great benefits, in a short space of time, to the military electronics community.

More power from boundary scan

However, to derive the greatest benefits from using this approach, military designers as well as commercial designers need powerful JTAG test tools that are easy to learn and use. In addition, boundary scan test gear can potentially extract a great deal of information about the unit under test by analyzing the responses of JTAG-compliant devices. User-friendly features, for example speeding up test compilation and supporting easy reuse of test scripts, will also help maximize test coverage, reduce development time, and minimize errors during test generation in the face of decreasing access for test fixtures, flying probes, or manual probing with a logic analyzer or oscilloscope.

Next generation JTAG tools, such as the XJTAG development system from XJTAG Ltd. of Cambridge, UK, support high-level languages for test generation, allowing tests to be easily compiled and also readily modified, for example, in response to design changes. Enhanced graphical tools also allow engineers to view the states of individual pins in real time and to group and monitor sets of pins as a bus.

High-level test development

Without these capabilities included in the test tool, engineers must work hard to construct a suitable binary test sequence to exercise all the devices in the JTAG chain. In addition, a change to the board – such as adding or removing a component from the chain or moving a component to a different location by altering the routing – would require a new JTAG sequence. Hence, the most basic implementation of boundary scan implies a *board-centric* view of test compilation.

However, the XJTAG system was one of the first tools powerful enough to abstract engineers from the level of the JTAG bitstream and make JTAG easier and more intuitive to use. Instead of constructing the bitstream from the ground up, as it were, tests are now compiled automatically from input data that includes CAD netlist information and a test script for each non-JTAG device attached to devices in the JTAG chain. In this way, tests can be quickly recompiled following any change to the board layout, and test scripts can also be saved and reused on other projects because they are specific to the device. This is a *device-centric* use of JTAG and allows boundary scan testing to become much more powerful as well as easier to use.

Reusable tests

Since device-centric tests can be reused in future tests written for any board using the same device, engineers can save time and avoid potential errors. Organizations can build libraries of proven test scripts that can be readily incorporated into new routines. Figure 2 shows a sample test for a 90-pin BGA SDRAM device written in a high-level language.

In addition, non-JTAG devices that connect to JTAG-compliant devices can also be tested because the XJTAG system can

```
Test(){INT result}

  INT returnCode;

  PRINT("Checking ", SIZE_MB, " Mbyte SDRAM (", DEVICE_REF, ")\n\n");

  IF DEBUG THEN
    PRINT(DATA_PINS,    " data pins\n");
    PRINT(ADDRESS_PINS, " address pins\n");
    PRINT(DQM_PINS,     " DQM pins\n");
    PRINT(BANK_WIDTH,   " bank pins\n");
  END;

  PRINT("Initialising SDRAM...\n");
  result := RESULT_PASS;
  Initialise();

  PRINT("\nTesting ", DATA_PINS, " data pins... ");
  TestData(){returnCode};
  result := result | returnCode;

  PRINT("\nTesting ", ADDRESS_PINS, " address pins... ");
  TestAddress(){returnCode};
  result := result | returnCode;

  PRINT("\nTesting random data/address... ");
  TestRandom(256){returnCode};
  result := result | returnCode;

  Initialise();

  IF (result = RESULT_PASS) THEN
    PRINT("SDRAM tests passed.\n");
  ELSE
    PRINT("SDRAM tests failed.\n");
  END;

END;
```

Figure 2

automatically calculate which JTAG pins need to be manipulated in order to access those nets.

Development and production roles

To execute a boundary scan test, whether generated manually or automatically by a tool such as XJTAG, the board does not have to be running. This makes it a powerful technique for development engineers, who can use it to quickly verify basic functionality as soon as the first prototypes return from assembly. The time-consuming process of debugging the processor or memory system and problems that will prevent the board from booting up at all can be quickly pinpointed.

Modern JTAG tools also provide a convenient means to toggle individual pins or buses and view pin states on screen to quickly locate bridges, breaks, poor joints, or incorrect connections. The screenshot in Figure 3 demonstrates viewing the status of all BGA and fine-pitch leaded device I/Os. This can be accomplished more quickly than laboriously checking using a continuity tester, even assuming that sufficient physical access is possible. The results are also readily recorded for future reference. Users can also quickly and easily repeat any or all of the tests for a board, to enable them to track down a fault.Another benefit is that test development can begin concurrently with prototype debugging, and production tests can be quickly finalized when the design is fixed. In this way, Design For Test (DFT) becomes more intrinsic to the project.

Programming with JTAG

Another feature of boundary scan or JTAG testing is the ability to program devices such as CPLDs, MCUs, or flash memories by shifting in the required bits using the JTAG chain. But there is even greater power and flexibility to be gained by communicating via the JTAG port of compliant devices in yet more sophisticated ways. For example, given suitably powerful tools, it is possible to

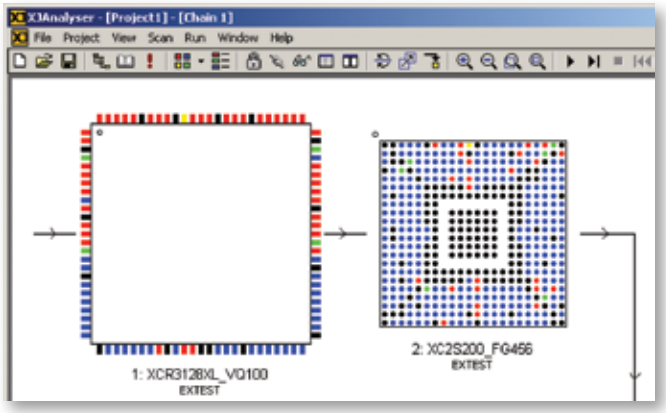

Figure 3

step through or over test code a line at a time while controlling the device through the JTAG port. Break points can also be created and edited, and the values of variables in the code can also be checked or modified.

Modern JTAG equipment in practice

Thales UK has used the XJTAG Development System as the basis for a common DFT strategy spanning development, first article build, production, and field service. The first project to benefit from this tool was the Thales MSN 8100-H, Europe's first operational Software Defined Radio (SDR), which will be used on the Royal Navy's next class of Destroyers, the Type 45, scheduled to enter service in 2009. Figure 4, provided by BAE Systems, shows an artist's impression of the Type 45 Destroyer. During development of signal processing boards for this SDR, engineers saved around 20 percent of debugging and testing time by applying boundary scan testing using the XJTAG system.

The MSN 8100-H signal processing boards are densely populated and use fine-pitch, high-density connectors as well as FPGAs in high-I/O BGA packages. These make the boards difficult to test by traditional methods. According to engineers at Thales, the number of JTAG-compliant devices per board has been steadily increasing with each new project. On the MSN 8100-H project, there were enough to use the JTAG chain for debug and testing. Thales was very quickly able to establish test coverage of around 80 percent. Fault-finding capabilities also proved effective, such as circuit visualization tools that allow reading and writing to all of the JTAG pins in the chain and display the status of each pin graphically.

Using JTAG, the engineers at Thales UK were able to begin test development and design validation of CAD netlists at a much earlier stage in the project. In addition, the ability to quickly generate complex functional tests also helped shorten the time for development and first article build. Because the tests are automatically compiled using scripts specific to each device, a script can be reused any time that device is used, whether this is at other locations on the same board or on a completely different board. The scripts are also portable to other projects.

Military response unavoidable

The test challenges facing commercial equipment designers are now hitting home in the military sector. Increasing board complexity and difficult physical access are forcing adoption of new test techniques in order to maintain coverage. Solutions that continue to depend on physical access have only a limited lifetime before the number of accessible pins and test points becomes inadequate to sustain test coverage. With the number of available JTAG-compliant components increasing steadily, as well as the advent of enhanced boundary scan test equipment, migration to JTAG testing is another commercial trend the military is likely to adopt in the near future.

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Figure 4

