The potential of boundary scan

By Dominic Plunkett

Debug and test techniques must advance in parallel with new design approaches being applied at component and board levels.

Trends such as the increasing adoption of BGA devices, chip-scale packages, multi-layer board design and high-speed signalling reduce the test coverage achievable using conventional probes or fixtures.

Pressure to increase productivity is also sharpening focus on the time necessary to test, or locate a fault.

Boundary scan testing presents an answer to the progressive designing-out of test access. It also has the ability to establish a deterministic test duration for a board, for all stages of the product lifecycle.

Boundary scan test equipment with graphical user interfaces has allowed engineers to access more of this technology's potential. Boundary scan allows engineers to manipulate and query the internal circuitry of components on the board, to verify devices are functioning correctly and are connected properly.

Available tools automate test-sequence generation by combining the board netlist with data about the individual components to be tested.

A high proportion of the circuit - devices with integrated boundary scan circuitry and non-compliant devices - can be tested.

Hence, boundary scan testing can be applied to components including SDRAMs, Ethernet
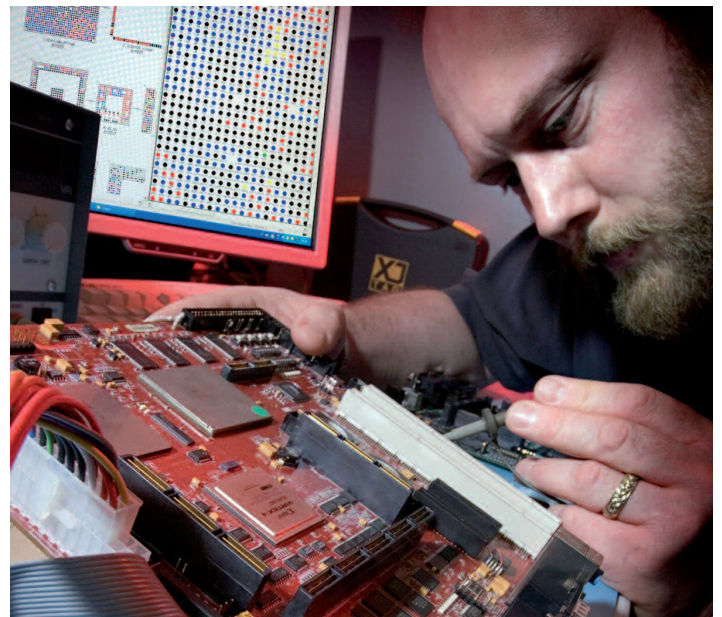
Andy Evans, senior product engineer platforms at the Systems Design Division ARM using XJTAG.

controllers, video interfaces, flash memories, FPGAs, microprocessors and others. The boundary scan chain also supports in-system programming of FPGAs, CPLDs and flash memories.

The test-access and test-duration challenges have been key drivers for the adoption of boundary scan testing for development as well as production. ARM, for example, is using the XJTAG boundary scan system to test boards for its RealView processor development platforms.

With tens of thousands of pins on each board, engineers identified boundary scan as the only means to validate this circuitry in a commercially realistic timescale. XJTAG has enabled ARM to accelerate debugging and testing, to increase test coverage to 90 per cent and significantly improve production yields.

ARM has been able to apply boundary scan from the very beginning of the development process to help improve the design and reduce re-spins. By automatically adapting to design changes reflected in the netlist, the system saves engineers from manually picking through the netlist for errors.

The future promises even greater use of boundary scan technology. Not only are more boundary scan compliant devices entering the market, but IC designers are using the circuitry to provide access to new and innovative on-chip features. Boundary scan has the potential to further increase test coverage and support additional test modes without requiring extra physical access.

Dominic Plunkett is chief technology officer at XJTAG