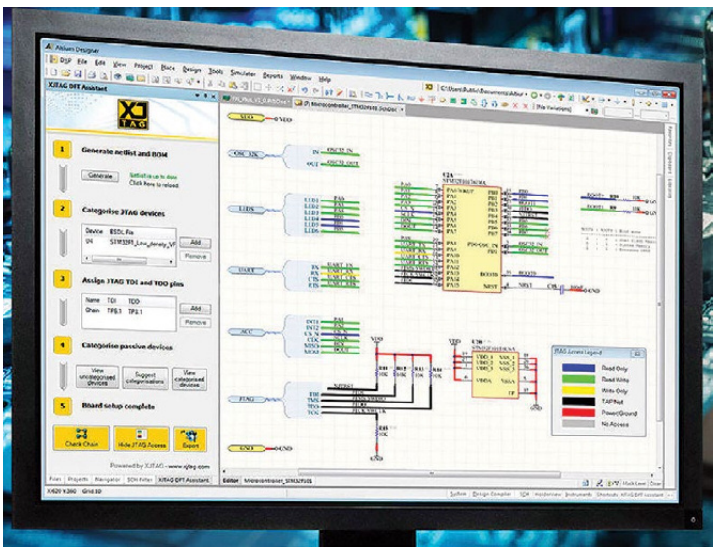
DESIGN

Tool tests JTAG scan chain coverage for PCB designers

Boundary scan chain integrity can be checked automatically on Altium's Designer schematic capture and PCB layout software, using an extension from Cambridge-based XJTAG.

Called XJTAG DFT Assistant, and downloadable for free, it "provides engineers with an extension to check if boundary scan chains are correctly connected and terminated at the schematic capture stage, long before the PCB is produced," said XJTAG CEO Simon Payne.

"While the first prototype is being manufactured, XJTAG DFT Assistant allows you to export a preliminary XJTAG project from Altium Designer to the XJTAG development software, where additional tests can be developed. These can then be used to test real hardware, as soon as it's available," said Payne.



The assistant uses a 'Chain Checker' and an 'Access Viewer'. Chain Checker identifies common errors in a JTAG scan chain, such as incorrectly connected test access ports (TAPs), where a single connection error would stop an entire scan chain working. Incorrectly terminated TAPs are also identified.

Access Viewer overlays the extent of boundary scan access onto the schematic diagram, allowing users to instantly see which components are accessible using boundary scan and, more importantly, which are not.

Boundary scan (IEEE 1149.x) gives serial access to all pins (or leads, pads or balls) on a chip package, allowing all connections into the chip to be exercised or probed, and all PCB traces and circuits connected to the chip to be exercised or probed. A four or five-signal bus sequentially connects JTAG-enabled devices, looping from chip to chip.

"Useful from prototype bring-up to production test, boundary scan allows a wide range of faults to be detected, such as short circuits, open circuits, stuck-at high/low faults and missing pull-up/down resistors," said XJTAG, whose products develop suites of boundary scan tests from design data.

www.xjtag.com

MICROPROCESSORS

USB bridge chip supports USB2.0

FTDI Chip's latest USB bridge ICs support USB 2.0 Full Speed (12Mbit/s).

Available in 28-pin SSOP and 28-pin QFN package options, they have dual human interface device support, with I²C and UART bus conversion capabilities.

The FT260 runs the USB protocol and standard class drivers. IO is compatible with 1.8V to 3.3V systems.

During full operation only 24mA of current is drawn, which falls to 385uA in suspend mode. The FT260 is the first device of its kind to be compliant with the HID-over-I²C protocol specified by Microsoft in the release of Windows 8.

Four speed-modes are avaialble in I²C bus: standard mode, fast mode, fast mode plus and high speed with 7-bit addressing supported.

www.ftdichip.com/ft260

PROCESSOR

Wireless baseband processor for LTE small cell networks supports 2Gbit/s

Lattice Semiconductor has introduced a baseband processor for wireless access and wireless backhaul LTE small cell networks operating in the 60GHz band.

Lattice also offers the Sil6340 and Sil6342 60GHz RF transceivers.

The chips support beam-steering technology on phased array antennas.

Devices that implement beam-steering require only rough alignment and can be installed quickly without specialsed skills.

A link can then be established between that node and other nodes in the network without manual intervention, and maintained even under changing environmental conditions or network reorganisation. The SB6541 baseband processor supports internet protocol (IP) data rates of up to 2Gbit/s, with a typical throughput of 1Gbit/s at a range of up to 300 metres. The device integrates with the RF transceiver via high-speed analogue I/O and a digital control interface.

www.latticesemi.com