MEMORY

ST embeds 55nm flash in MCUs

STMicroelectronics is integrating embedded flash memory fabbed on a 55nm process in its next-generation automotive microcontrollers due next year.

The company currently integrates 90nm embedded flash in its automotive microcontrollers but says power and performance requirements are outpacing what 90nm-based chips can deliver.

The 55nm process is in production at its facility in Crolles, France.

Infineon and TSMC are also co-developing 65nm process technologies for eFlash microcontrollers for the car, chip card and security markets.

www.st.com

TEST

Imagination at the boundary

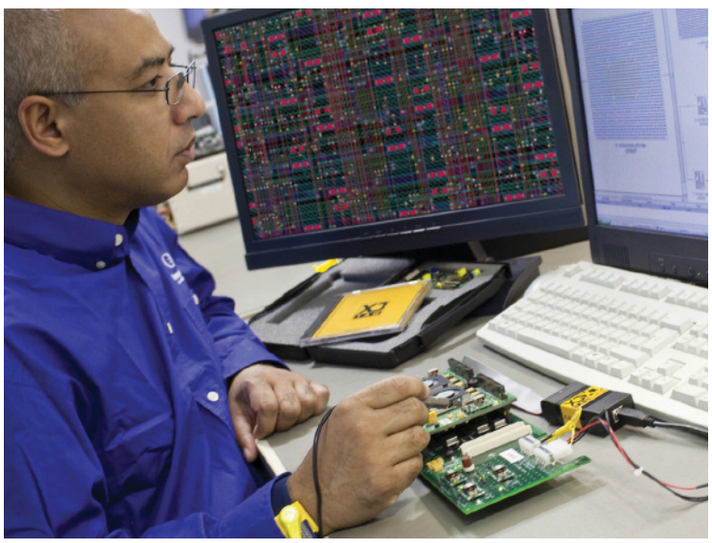
Imagination Technologies has opted for an Xjtag boundary scan system to test and debug its multimedia system-on-chip devices.

"We recognised the need to move from socket-based testing to a boundary scan-based system," said Mark Dunn, vice-president of engineering at IMGworks in Hertfordshire.

Boundary scanning is used to test and debug prototypes, test assemblies and customer development boards. It allows for the compilation of effective test scripts even before the hardware is ready.

"The system has much greater functionality than we expected. We can test memory interfaces and non-JTAG components well beyond the scan chain, making it very flexible for debugging in the lab," said Dunn.

www.xjtag.com



DESIGN

Toshiba foundry offers 180GHz RF, 40nm CMOS

Toshiba is offering Europe RF chip designers a foundry service for system-in-package (SiP) devices with integrated radio frequency circuits and digital CMOS down to 40nm process nodes.

For the RF process design kit, 130nm, 90nm and 65nm processes are characterised by transistor F(t)s of 90GHz, 140GHz and 180GHz respectively.

The RF chip will include passive elements such as MIM capacitors.

It will also have junction and mosfet varactors (deep N-well, single-end and differential) and half-turn differential or symmetrical inductors, as well as mid-range polyresistors with zero temperature coefficients.

Junction capacitors and parasitic devices such as NPN transistors are also available.

To support chip development, Toshiba is offering a hybrid model flow which includes the digital baseband processor and the other for the analogue and RF elements.

For the RF and analogue elements, the customer implements the GDSII based on the RF-PDK.

Once the macro cell layout is frozen, all manufacturability and yield-assurance rules will have been followed, and downstream respins avoided.

For the digital portion of the chip, an RT-level or gate-level netlist is accepted. The GDSII for the digital portion is implemented by the foundry, as in a standard Asic flow.

Standard Asic libraries, SPICE DFM/DFY models and package parasitics are part of the design environment. The analogue or RF blocks are finally integrated into the top-level layout.

After the SoC layout is complete, the customer signs the project off based on the verification reports provided.

www.toshiba-components.com

Also see on our website: ElectronicsWeekly.com
IMEC teams with Renesas for 40nm CMOS RF transceiver
http://tinyurl.com/yejksbg