MILITARY OPTS FOR JTAG TEST COVERAGE

New JTAG tools that extend boundary scan test capabilities can help military designers meet the test access challenges that come with the most advanced COTS silicon

The test challenges facing designers of commercial equipment are now affecting the military sector. Increasing board complexity and difficult physical access are forcing the adoption of new test techniques in order to maintain test coverage. Solutions that continue to depend on physical access have only a limited lifetime before the number of accessible pins and test points becomes inadequate to sustain test coverage.

The use of leading-edge COTS (commercial-off-the-shelf) semiconductor components achieves high performance targets within tight time constraints, particularly for network-centric and C4ISR (command, control, communications, intelligence, surveillance and reconnaissance) applications.

To achieve the full benefits, such as high performance video and graphics manipulation, as well as intensive data and signal processing, designers need to use the highest performance commercial silicon available. As a result, modern military boards increasingly feature powerful commercial DSPs, large FPGAs and dedicated video and graphics processor chips, as well as high performance standard products.

Defence equipment designers also face tight development and delivery schedules. However, testing becomes more difficult as COTS silicon tends to come packaged using commercially efficient technologies, including BGAs and ultra fine pitch QFPs. These allow densely populated boards and large numbers of inter-IC and off-board signals. However, direct access to individual device I/Os is impossible.

Additionally, many signal paths never reach the surface of multi-layer military PCBs. Adding vias to bring signals to the surface increases the cost and complexity of board routing and fabrication. In addition, the sheer number of high performance COTS components mounted on each board, which support the functionality required to react in real time to vast quantities of incoming sensor and command data, restricts potential test point locations on the board surface. High signalling speeds and high operating frequencies also discourage the use of additional PCB tracking to reach test points.

Boundary scan testing allows engineers to locate faults within minutes that may take several days to locate using traditional test techniques

All of this prevents attachment of test probes, which tends to restrict coverage and fault diagnosis using traditional techniques such as flying probes, logic analysers, and oscilloscopes. The disadvantages are evident during production testing, as well as on the developer's bench and in the field. Military electronics designers are increasingly turning to solutions which use boundary scan and do not require physical access to chip I/Os or test points.

Test without probes

Boundary scan testing in accordance with IEEE1149.1 (JTAG) circuitry to test connectivity and functionality is integrated onto the silicon of individual components. External pins and boundary cells create a JTAG port, through which the device can be stimulated and the responses collected.

Serially linking the ports of all JTAG-compliant devices on the board creates a JTAG chain. A test pattern can then be shifted into and out of each device to test connectivity and functionality, without requiring probes to be attached to individual device I/Os to monitor responses. Connecting the JTAG chain to the test system through a single on-board connector allows a high level of test coverage, even when high component density, COTS package styles and multi-layer board design preclude physical access to the majority of inter-IC signals.

The number of JTAG-compliant COTS and custom ICs available, including military

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qualified components, is increasing. For instance, microprocessors and microcontrollers routinely provide a JTAG port to support various debugging tools. FPGA manufacturers have also identified JTAG as a convenient means of verifying the device at relatively low cost in terms of silicon real-estate and device I/O.

FPGA verification and debugging tools such as Xilinx ChipScope Pro, which uses the JTAG interface to access internal signals and nodes within the FPGA, allow designers to allocate more pins to functional I/O, rather than debug. Designers of many standard ICs are also implementing JTAG on-chip as a solution to the growing challenges to test access.

With more JTAG devices on each new board, the number of components and functional nets that can be tested via the JTAG communication port also increases rapidly.

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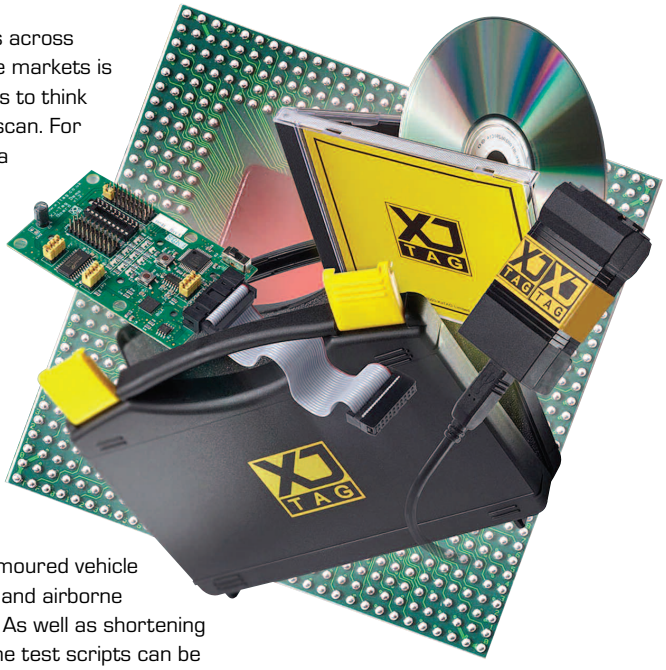
As an example, Thales UK uses XJTAG's boundary scan development system to debug and test complex PCBs in its software-defined radios (SDRs). The system debugs and tests the baseband PCBs that form part of the MSN 8100-H SDR, European operational software radio. The radio is designed for naval and ground-based applications and is on the Royal Navy's next class of Destroyers, the Type 45, scheduled to enter service in 2009. An artist's impression of the Type 45 Destroyer, provided by BAE Systems, is shown on page 23.

The SDR baseband boards are densely populated and use fine pitch high density connectors, as well as large and expensive BGA/FPGA devices, all of which make the boards difficult to test by traditional methods. The boundary scan system has enabled Thales to cut the development time for debugging and testing boards by around 20 per cent and it has provided the basis for a common design for test strategy, spanning development, first article build, production and field service.

The increasing deployment of FPGAs and other JTAG-enabled ICs across aerospace and defence markets is forcing board designers to think again about boundary scan. For example, engineers at a COTS embedded solutions supplier are using XJTAG to debug and test a graphics and imaging platform.



The new board , which features a high-performance FPGA, is designed for use in military and C4ISR applications including naval consoles, rugged vehicles, unmanned armoured vehicle (UAV) ground stations, and airborne command and control. As well as shortening debug and test time, the test scripts can be re-used by the contract manufacturing partner for production testing.

Troubleshooting

The use of scripts for individual devices mean that tests can be quickly re-compiled following changes to the board layout. Device scripts can also be saved and re-used on other projects; they are specific to the device, not the board. Engineers can build libraries of proven test scripts to save time and reduce errors.

Powerful graphical capabilities are also becoming increasingly important in emerging JTAG equipment, to help engineers analyse test results. The XJTAG GUI, for example, displays the states of individual pins in real-time, and allows the user to toggle selected pins and view responses, and to group and monitor sets of pins as a bus displaying binary or hexadecimal values.

Boundary scan testing using XJTAG allows engineers to locate faults within minutes that may take several days to locate using traditional test techniques, and may even prove impossible to find. This demand for fast and deterministic troubleshooting is another aspect of commercial product development that is becoming increasingly prevalent in the military domain.

In addition to its development role, JTAG is increasingly being used in production testing,with other test and development equipment, to maximise test coverage. XJTAG integrates easily with larger test routines written in C or Visual Basic, for example. The main application can call up an XJTAG script without requiring an API call, and the results can be used directly for validation and reporting.

This allows a composite test strategy, using JTAG for inaccessible nets, and traditional functional and in-circuit testing for passives and accessible components. However, by using JTAG to perform a higher proportion of these latter tests too, hardware test fixtures can become even simpler and less expensive. For example, using XJTAG with the optional XJIO board, digital and analogue signals can be verified right through to the external connections. Basic analogue measurements, such as testing that a power rail is within limits, can also be controlled via the JTAG interface, extending JTAG to address testing COTS components in military systems.

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