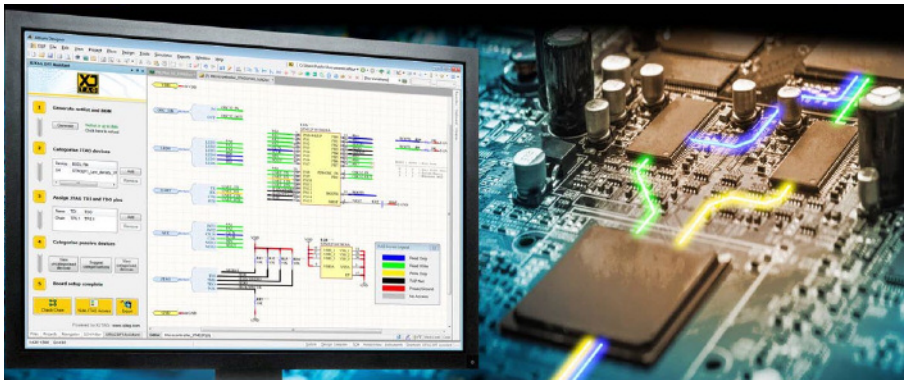
Making design-for-test a push-button process

By Philip Ling

Implementing a Design for Test approach when designing PCBs at the schematic capture stage can now be significantly assisted using an innovative and free software extension that adds design verification to Altium Designer.



The concept of 'right by design' could imply that the design in question will always work as expected, so there is no need to test it once it has been designed 'right'. While this is true, in principle, it is also true that testing isn't primarily a process of finding design faults; that's a development issue.

Although there is always the potential for new 'bugs' to appear at any time, faults that appear after the design phase is complete, particularly in mature products, are likely to be the introduced by the manufacturing process. The list of potential manufacturing defects that can occur in a wave soldering process, for example, is long and includes: incomplete joints; dry, cracked or bulbous joints; lifted pads or resist; pad contamination; solder balling and, of course, open circuits and solder shorts.

Any of these defects can stop a board from working and some may not become apparent until long after it has been shipped. Adopting a Design for Manufacture (DFM) approach can help minimise the occurrence of these types of defects and these are measures that are normally best applied at the PCB layout stage. Modern design tools can help automate this by imposing design rules during this stage, for example.

Despite how well a board is laid out, manufacturing defects are inevitable and so need to be found before the product is shipped, during the test process. Adopting a Design for Test (DFT) approach can ensure that detecting and locating manufacturing defects is possible, even faults that are located beneath surface mounted devices. Rather than strict design 'rules', such as minimum spacing between tracks, or routing on specific layers, DFT involves approaches that need to be more widely adopted earlier, and implemented at the schematic capture stage.

DFT, right by design

Designing for test is, perhaps, more subjective than designing for manufacture. What may be right for one design may not be right for another, due to cost, space or complexity constraints. What is almost uniformly agreed amongst IC manufacturers, however, is that including a DFT technology such as Boundary Scan in complex integrated devices is now the norm.

While JTAG is often used to debug software running on a microprocessor, boundary scan has far wider application. It was developed to address the challenge of finding manufacturing defects 'hidden' beneath advanced surface mount components (typically Ball Grid Arrays, or BGAs).

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It offers a level of test access that is significantly greater and more cost-effective than many other forms of test and, perhaps even more significantly, because it is 'built-in' to devices it doesn't impose a premium on the cost of those devices. Most FPGAs/CPLDs and processors (including microcontrollers), as well as some fixed-function parts such as Ethernet transceivers, interface controllers and PCI Express PHYs now implement boundary scan.

Accessing boundary scan functionality in a manufactured product requires the right specialist hardware and software, but ensuring your design is ready to offer that access is free; it simply requires a Design for Test approach at the schematic capture stage of development. Attempting to implement or correct a boundary scan chain during or after PCB layout is effectively futile; making sure it's right by design during schematic capture is simpler and, therefore, much more cost effective.

Getting the scan chain correct

Boundary scan is implemented using a dedicated bus, which comprises between four and five signals. These signals, collectively referred to as a Test Access Port, or TAP, need to be correctly connected to all JTAG-enabled ICs in a daisy-chain configuration, known as a scan chain. The TAP is routed from a connector to the first IC in the scan chain and then on to the next and so on, all the way to the last IC in the chain and back to the connector.

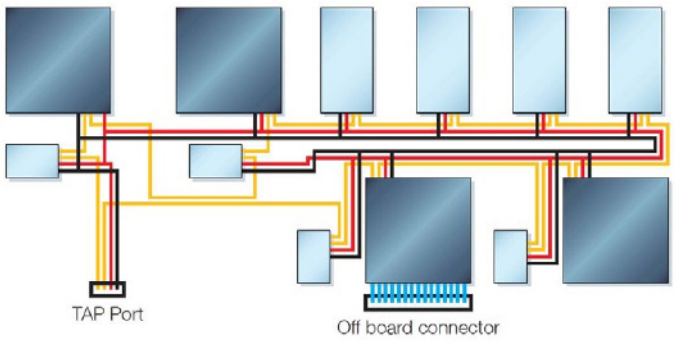

Fig. 1: The boundary scan chain sequentially connects JTAG-enabled devices on a PCB, enabling test access for running connectivity and functional tests.

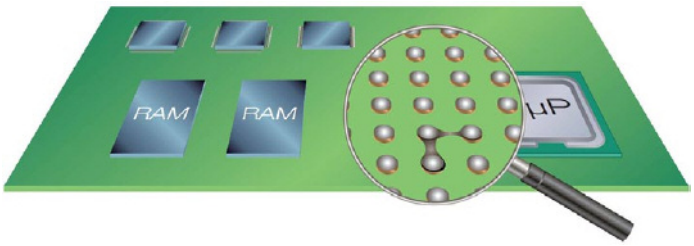

Fig. 2: Boundary scan allows manufacturing defects 'hidden' beneath BGAs to be located

The sequential nature of the scan chain means that the boundary scan test pattern must pass through each device and return to the connector. It is therefore imperative that there are no broken or weak links in the scan chain. This introduces a number of DFT considerations, such as ensuring the scan chain is connected to every JTAG-enabled IC in the design, that the chain's TAP signals are correctly connected to the right pins on those ICs and that the recommended termination is used on the TAP signals.

As well as defining the electrical characteristics of the TAP, the IEEE 1149.1 (boundary scan) standard defines the scan chain's protocol. This enables the identification of devices, the pins used for the TAP and the test capabilities that device supports. This information is stored in a dedicated file known as the Boundary Scan Description Language file (BSDL); every IC that is JTAG-compliant must have a BSDL file associated with it. The information held in this file enables specialist software and hardware providers to create the products used to access and control JTAG-enabled devices during test.

Automating DFT

Checking that all JTAG-enabled devices in a scan chain are connected correctly is normally a manual process and therefore just as susceptible to human error as any other manual design process. But it has recently become possible to automate the design verification of a boundary scan chain. Using its expertise in boundary scan testing, XJTAG has developed a free software extension for Altium Designer that assists with the design verification of a boundary scan chain, enabling a new level of DFT capability to the environment.

The extension, called XJTAG DFT Assistant, uses the netlist generated by Altium Designer during schematic capture to form a profile of how the scan chain is connected in the design. This picture is complemented by importing BSDL files to the project, allowing it to understand how the scan chain should be routed. From here the extension is able to not only check the connections of the scan chain in the schematic but also show the level of test access the design offers to boundary scan software/hardware.

The extension achieves this through two main features; the XJTAG Chain Checker and the XJTAG Access Viewer. The data collated can also be exported for use in XJTAG's boundary scan test development environment, XJDeveloper. This supports the development of boundary scan tests for both JTAG-enabled and non JTAG-enabled devices. It is possible to extend test access to a larger percentage of the circuit if it is designed with boundary scan testability in mind. Using the XJTAG Access Viewer feature, designers can monitor, evaluate and maximise their test access at the schematic capture stage, something that couldn't be automatically verified before the introduction of this free software extension.

Crucially, the extension is also able to detect errors in the scan chain long before the PCB moves to the layout stage.

By making it part of the design process, the XJTAG DFT Assistant can help designers avoid the common faults that would normally inhibit a scan chain from working, such as incorrectly routed TAP signals or poorly terminated signals. Perhaps more importantly, it shows the board designer which ICs are accessible to boundary scan testing, thereby highlighting any ICs that should be connected and aren't, or areas of a design that are currently inaccessible to boundary scan testing but could be, by making some design changes.

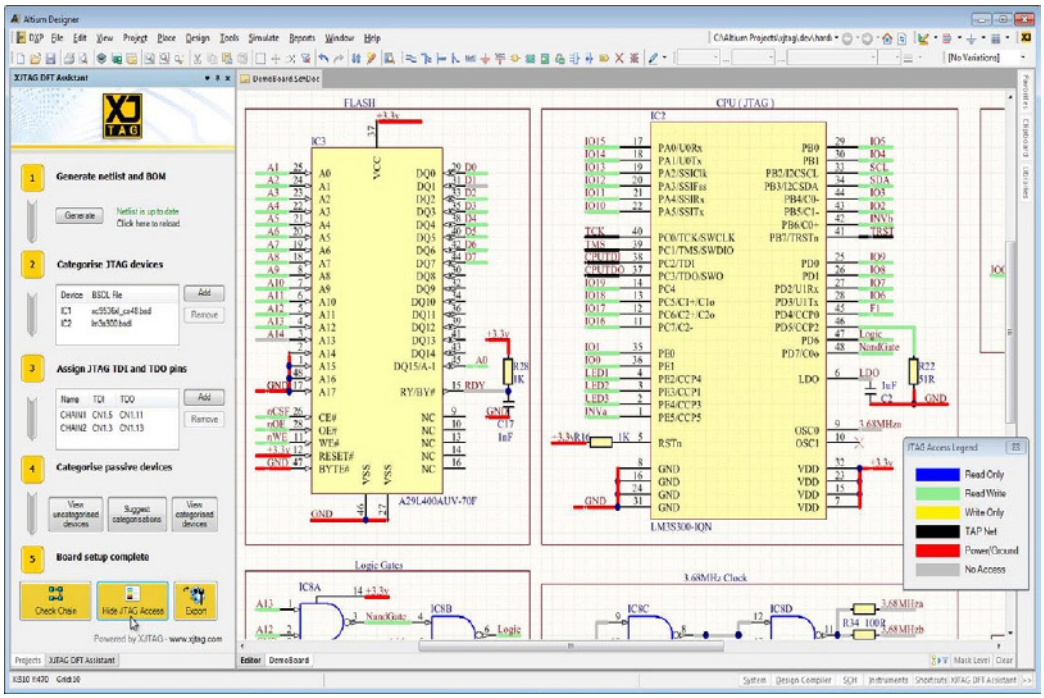

Fig. 3: The XJTAG DFT Assistant's Access Viewer mode clearly displays the level of test access available, allowing board designers to maximise test access at the schematic capture stage of design, long before moving to PCB layout.

These features can be used iteratively as the design evolves, ensuring that test access is maximised and that the boundary scan chains are right by design. Having this information at their fingertips will not only make developers more aware of how to implement boundary scan, but help automate the entire DFT approach to schematic design.

Understanding boundary scan and BSDL files enables specialists like XJTAG to develop the software and hardware products needed to use boundary scan throughout a product's life-cycle, from prototype bring-up to volume production.

By applying this expertise to develop a free software extension for Altium Designer, developers now have access to a powerful design verification technology that greatly increases their ability to get it right first time.