Boundary Scan Techniques for **Test Coverage Improvement**

When discussing the JTAG protocol, most engineers immediately think of In System Programming procedures. Indeed, there are numerous Microcontrollers (or FPGAs, CPLDs) that employ this protocol when it comes to their programming and such applications are widely spread throughout the industry. The fact is that this protocol can be also used for different other purposes which can strengthen your testing techniques. Boundary Scan testing (sometimes called JTAG testing) methods can significantly help you improve the TC (Test Coverage). This paper presents dedicated hardware and software tools which are focused on performing Boundary Scan (BS) testing. Additionally, some basic principles of the 1149.1 standard are described.

Introduction

In the last decades we have witnessed the proliferation of SMDs which incorporate increasingly complex functions into more and more reduced package sizes. This trend translates into integrating more devices on a smaller PCB area, fact which raises numerous test access issues. The challenge is to be able to adapt the test techniques to customer requests taking into account more and more I/O pins, less inter-pin spacing or sometimes no access to inner pins (in the case of BGA devices).

In the late 1990s the **JTAG** (Joint Test Action Group), composed of important electronics manufacturers, have promulgated the IEEE 1149.1 standard. This standard sets the rules and procedures for implementation of Boundary Scan techniques. Several other standard revisions have been adopted since then (like 1149.6 or 1149.7). Shortly said, using non-invasive testing, BS can help you obtain the following benefits:

- On each accessible net detection of Shorts, Opens, Missing Pull resistors, Stuck at 0 or 1.
- Testing of Microprocessors, FPGAs, CPLDs and other JTAG enabled devices.
- Testing of memory devices like DDRs, SRAMs, SDRAMs, Flash or EEPROMs.

- Testing of different other categories of devices like sensors, ADCs, Oscillators, Logic Devices, Serial Devices, Switches, LEDs and so on.
- Implementation of classical programming algorithms.
- Fast and reliable execution of all BS tests which can determine an improved Coverage.

Two preliminary considerations must be known. The UUT must have at least one JTAG enabled device (usually Microprocessors) which can be seen as the entrance point for the test vectors or signals. Basically, your BS tool will send/read different test signals via this entrance point.

These signals spread throughout all accessible nets. Values on these nets will be modified, read, compared and finally test results will be evaluated. This allows the non-invasive interaction with all previously mentioned devices.

So your UUT must provide access (via TPs or Connectors) to the BS enabled device dedicated pins. Four mandatory and one optional signal constitute the connection between your BS test tools and the Test Access Port on the entrance device.

Next, for the JTAG enabled device, one should have the so called BSDL (Boundary Scan Description Language) file. This file is usually provided free of charge by the device manufacturer. The BS tools need this file for the software setup of the tests. This file includes info like the logical port description, pin mapping, device ID code and so on.

Consider Figures 1 and 2 as a summary of what has been discussed. These images are obtained courtesy of XJTAG (www.xjtag.com), a company which is specialized in BS tools and implementations.

Figure 1 presents the UUT defects which can be detected by the BS implementation. Notice that procedures for detecting these faults are automatically included by dedicated software within the so called Connection Test. This test checks all connectivity around the JTAG enabled device and evaluates if it is in accordance with the design specifications.

Figure 2 shows the classical architecture of the JTAG enabled device. The BS tools will use the Test Data In (**TDI**) to send the test signals to the UUT and the Test Data Out (**TDO**) to read the test signals from the UUT. The procedures are coordinated by the Test Clock (**TCK**) and the Test Mode

Select (**TMS**) pins. The optional Test Reset (**TRST**) might be used to switch the behavior of the device from normal operation mode to the BS test mode. Note that this device has the Boundary Scan Cells that are used to implement the test procedure. In normal operation these cells may be ignored, however when BS is active, the cells isolate the Core Logic from the I/O pins and the Boundary Scan Register takes over.

pendent, however data must be applied in parallel. Usually, the most common PCB architecture is similar to the one presented in figure 3. With this architecture all states of the BS components are manipulated at the same time.

Using the TAP Connector data will be serially shifted from one device to another. The BS Chain Test will consist in sending

The Pull resistors from figure 3 may be used as guidelines when developing the PCB design with JTAG test possibilities.
More intuitive, consider figure 4. This image presents the layout of the Alfa Test Demo Board ver.1. This PCB has been developed by Alfa Test and it is used for demonstration purposes in ICT, Flying Probe, Functional Testing, Optical Inspection, X-Ray Inspection and LCD
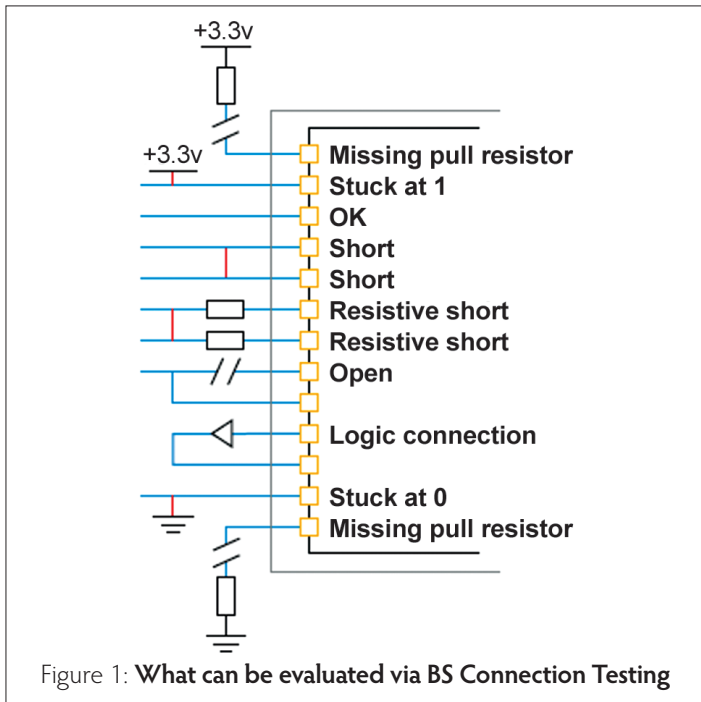

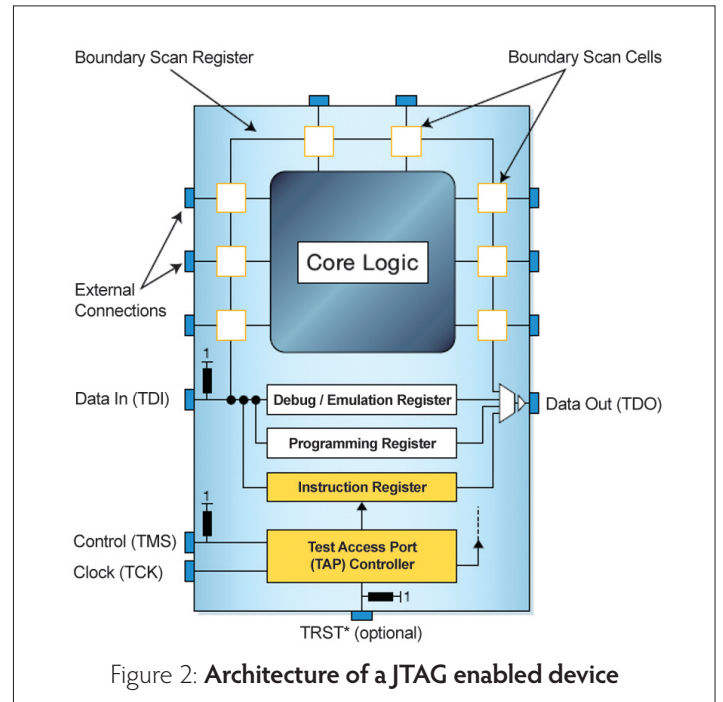Figure 1: **What can be evaluated via BS Connection Testing**

Figure 2: **Architecture of a JTAG enabled device**

How it works

The following paragraphs describe the way in which the implementation of BS testing works. Alfa Test is closely collaborating with XJTAG in order to deliver specific BS projects. So the recommendations which will be presented are based on our accumulated experience working and integrating XJTAG tools.

In principle, once the connection from the BS tools to the TAP (see figure 2) has been correctly set up, the BS Cells will be used as switches to pass data serially or parallel out and in the device which is tested. In this way, test vectors are shifted on all accessible paths from your PCB design. It is possible to have multiple JTAG enabled devices on an UUT. In this case one could create multiple scan paths in the sense that we are going to need multiple TDIs, TDOs, TMSs and TCKs. Also, according to your PCB design, multiple JTAG devices can share the same TMS and TCK signals. In this case we can say that the TDI/TDO signals are inde-
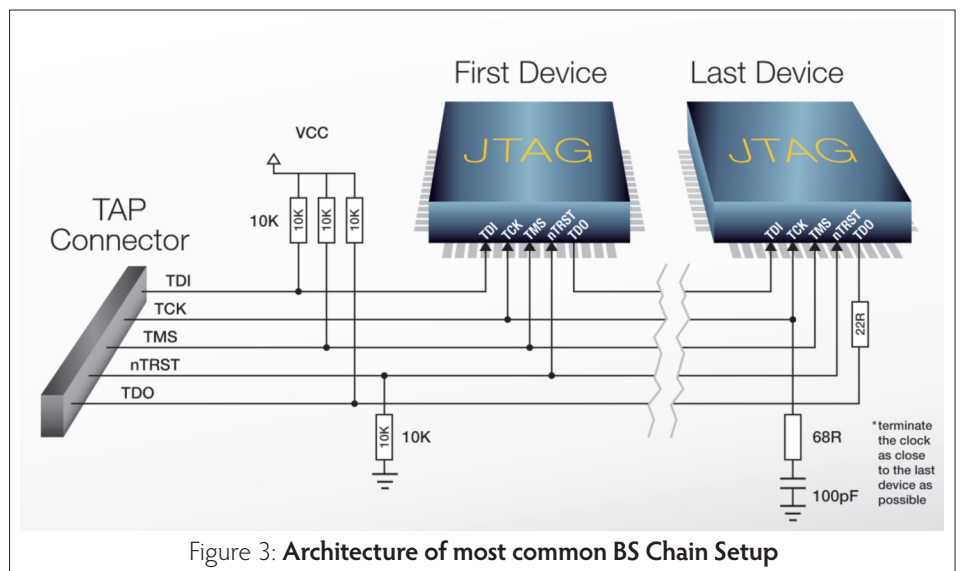

Figure 3: **Architecture of most common BS Chain Setup**

data from the TDI on the TAP Connector to the TDI pin of the First Device. Next, from the TDO pin of the First Device to the TDI pin on the Second Device and so on. Finally, the TDO pin of the Last Device on the PCB will return the test data to the TDO on the TAP Connector.

image inspection. An analogy with figure 3 is noticeable. Two JTAG enabled devices are included in the Chain. Device 1 is a XC2C256 BGA CPLD while Device 2 is an ATMEGA32 μC.
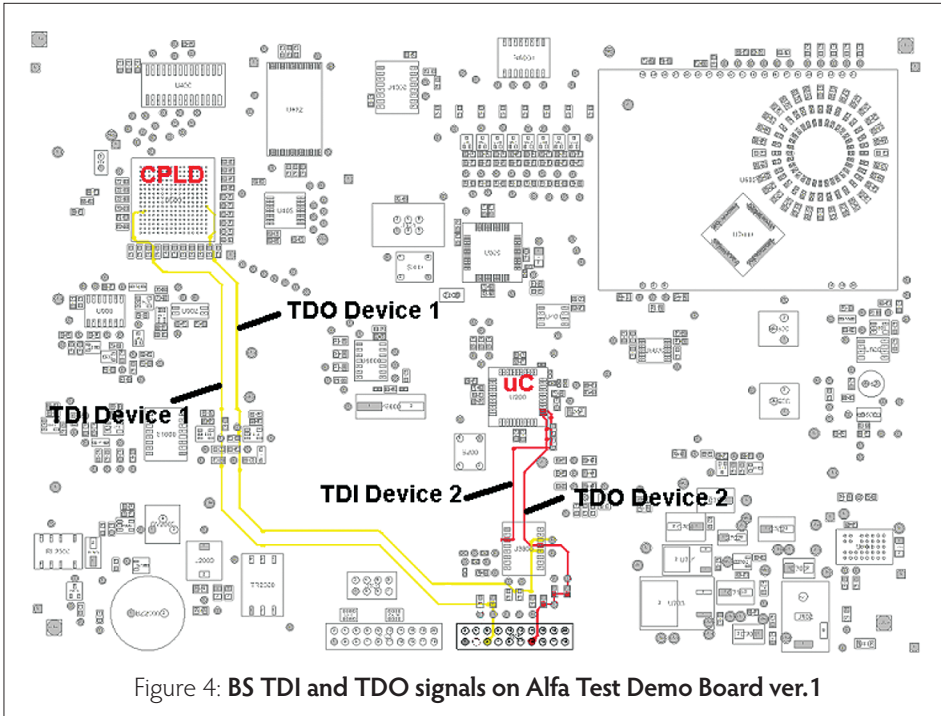These devices provide the access gates to more not JTAG enabled components. ➲

Figure 4: **BS TDI and TDO signals on Alfa Test Demo Board ver.1**

Either the USB or the PXI controller allows you to establish the connection to the TAP Connector of your UUT. This hardware communicates with the JTAG Chain and is used by the XJTAG Software Application. Basically, you need the XJLink2 to pass test data between your UUT and the software BS project.

In addition to the hardware, the software provided by XJTAG includes device drivers and a set of four base applications. Their description is presented in the following paragraphs.

The XJ Developer is the most complete package and allows the development of a BS project from start. This software requires some expertise in programming and hardware knowledge at component level. It automates a lot of the setup work and it is used to define the JTAG Chain, allocate the devices to be tested and obtain UUT coverage based on the schematics. So you actually don't need a physical connection to the UUT for obtaining the coverage.

The XJ Developer uses details from the Schematics, NetList, BOM and the BSDL files in order to setup the Chain and provide information about what can be tested and what cannot be tested. For testing non JTAG devices a library of already developed files is included. Latest updates to what devices can be tested are available on the XJTAG webpage.

So just by using the TAP port, via both JTAG enabled devices, a collection of other accessible devices can be tested (most important components being (SRAM, EEPROM, FLASH, ADC, LEDs, LOGIC Devices, Switches etc.).

Boundary Scan Tools and Examples

Over the past years Alfa Test has gained experience in working and developing BS solutions using XJTAG tools. Suffice to say that these projects can run in Functional Testing sequences or have been integrated in Keysight 3070 ICT.

At Productronica 2015, Alfa Test has presented a working solution which performs BS in the Takaya 9411CE Flying Probe system. This solution is still to be improved since due system, the latest of the series.

Different hardware tools are available on the XJTAG website, however we will refer to the XJLink2 controller which is available on both USB and PXI connectivity (see figures 5 and 6).

Figure 5: **XJLink2 USB connectivity with the host PC**

Figure 6: **XJLink2 PXI Chassis connectivity**

The XJ Runner is a tool which allows the user to execute projects already built by using the XJ Developer. So this tool does not allow project editing. It was designed

It can also be used to run SVF and STAPL/JAM files, files which can be built to execute a small program sequence using a JTAG enabled device.

Figure 7 presents a snapshot of the XJ Developer project Chain Setup for the Alfa Test Demo Board ver.1. Figure 8 presents the BS results after running a test on the XJTAG Demo Board v3.1. This shows how test results are displayed once a project setup has been completed.
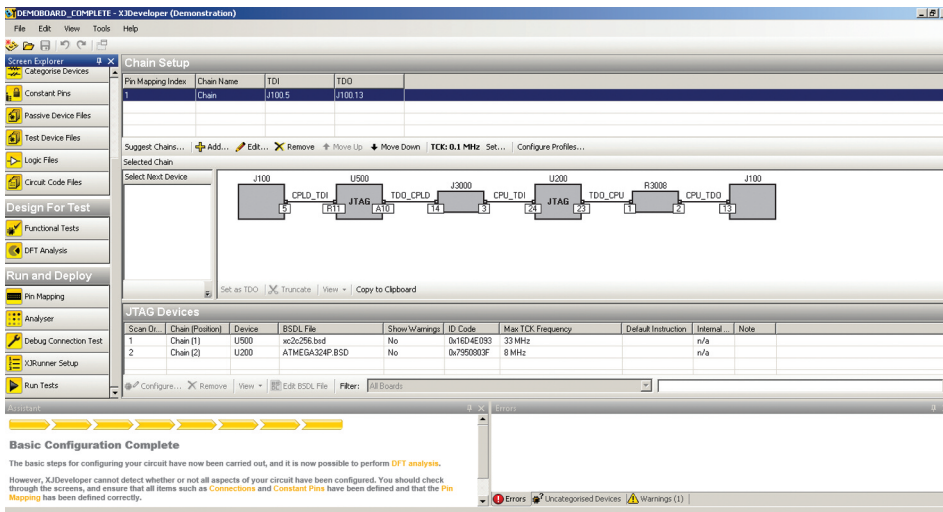
XJTAG projects can be called from LabVIEW/TestStand programs so the BS results can be included in such a test flow. BS data can also be transferred to text files so an analysis can be performed. The latest addition to the software packages is the XJ Flash which a specially designed tool for ISP programming for flash devices using JTAG protocol.

Figure 7: **XJ Developer Chain Setup Example on the Alfa Test Demo Board ver.1.**
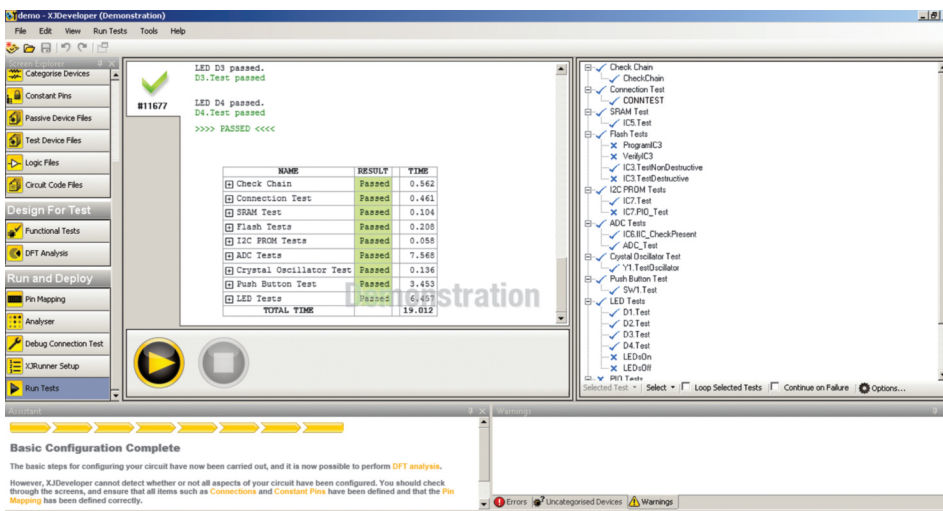
Figure 8: **XJ Developer test results on the XJTAG Demo Board Ver.3.1.**

Additional Information

This new technology for testing using XJTAG tools has gained increased interest over the past year. Finally, three important details should be mentioned.

First of all, at the event entitled Alfa Test Technology Days (April 2015, Timisoara, Romania), the XJTAG technology has been introduced and presented to over 15 test engineers from different companies acting in the electronics industry.

They have been able to see and work hands on with the XJLink2 and the corresponding software tools.

The success of Alfa Test with the integration of XJTAG tools in the Takaya 9411CE Flying Probe system has been confirmed at Productronica 2015 (November 2015, München, Germany). This shows the Alfa Test team competence when working with BS tools from XJTAG. ⮌

only for running the BS tests. It may be an option for customers that do not want to allocate time for studying how a BS project is designed and implemented. They are usually interested in running the project built by Alfa Test and testing their PCBs.

The XJ Investigator is used to detect and diagnose PCB problems. It is dedicated to the in depth analysis of whichever fault has been detected by running the BS tests.

Finally, the XJ Analyzer provides a tool which allows real time interaction between the user and the Chain components. It provides a graphical view of JTAG Chain. It facilitates complete control, pin-by-pin oriented, of both pin state (either driven as an output or tristated as an input) and pin value (either high or low when driven).

XJTAG BS Techniques Demo at Alfa Test Technology Days

XJTAG is currently supporting the Measurements and Optical Electronics Department – the Faculty of Electronics and Telecommunications from the University "Politehnica" from Timisoara. The company has facilitated the access of the students to XJLink2 complete kits, thus helping in the tuning of the educational process according to industry latest techniques.
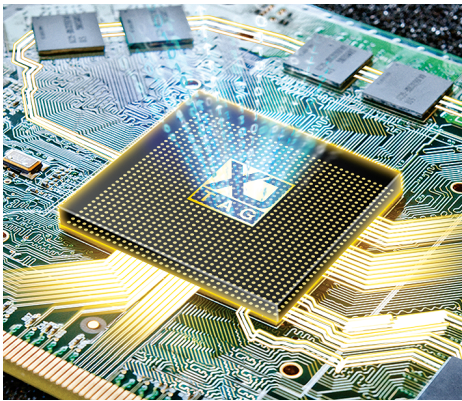
Takaya and Alfa Test members at Productronica 2015 – after BS integrated in the Takaya flying probe demonstration

As a conclusion, BS projects have been deployed with efficiency and are successfully used in production environments. A general view of XJTAG BS dedicated test packages is presented in Figure 9. For all inquiries and discussions please do not hesitate to contact the Alfa Test office. ■

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4th Year students working with the XJTAG tools, learning BS techniques

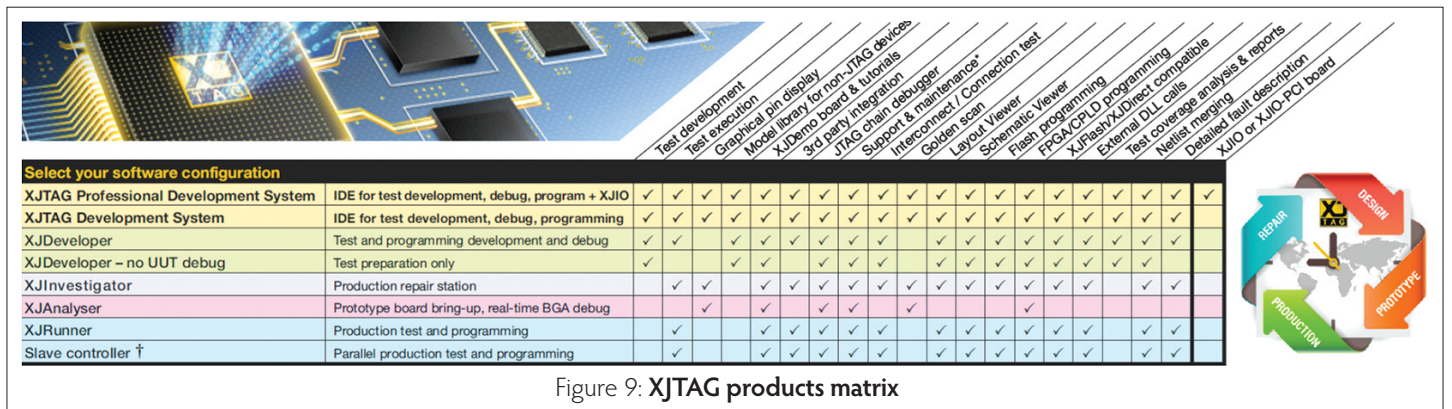| Select your software configuration		Test development	Test execution	Graphical pin display	Model library for non-JTAG devices	XJDemo board & tutorials	3rd party integration	JTAG chain debugger	Support & maintenance*	Interconnect / Connection test	Golden scan	Layout Viewer	Schematic Viewer	Flash programming	FPGA/CPLD programming	XJFlash/XJDirect compatible	External DLL calls	Test coverage analysis & reports	Netlist merging	Detailed fault description	XJIO or XJIO-PCI board
XJTAG Professional Development System	IDE for test development, debug, program + XJIO	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
XJTAG Development System	IDE for test development, debug, programming	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
XJDeveloper	Test and programming development and debug	✓	✓		✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	
XJDeveloper – no UUT debug	Test preparation only	✓			✓	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	
XJInvestigator	Production repair station		✓	✓		✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓		✓	✓	
XJAnalyser	Prototype board bring-up, real-time BGA debug			✓		✓		✓	✓		✓			✓							
XJRunner	Production test and programming		✓			✓	✓	✓	✓			✓	✓	✓	✓	✓		✓	✓		
Slave controller †	Parallel production test and programming		✓			✓	✓	✓	✓			✓	✓	✓	✓	✓		✓	✓		

Figure 9: **XJTAG products matrix**

Alfa Test is the regional distributor and integrator of the XJTAG boundary scan test platform in Romania, Bulgaria, Slovenia, Serbia, Croatia & Macedonia.